Question Paper

Exam Date & Time: 16-Jun-2023 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
END SEMESTER THEORY EXAMINATION - MAY 2023
II SEMESTER B.Sc (Applied Sciences) in Engg.
Switching Circuits and Logic Design [ICS 122]

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

Missing data, if any, may be suitably assumed

1) Simplify the following expressions using algebraic manipulation. (10)

i) f= x2x3'x4+x1x3x4+x1x2'x4
ii) f= (x1'+x2+x3). (x1'+x2'+x4'). (x1'+x3+x4) Find the minimum cost SOP and POS

expression for the following function using K-map and design the circuit using only NOR gates.

i) F(w, x, y, z)= ∑m(0, 1, 3, 4, 7, 11, 13, 15)+D(9, 12, 14)

2) Design and write verilog code for the following. (10)

i) 4-bit Adder/Subtractor.
ii) 3 to 8 Decoder with active high enable input and active low output.

3) Write down the implications of "delay issues" in 4-bit adder circuit and explain how it can be rectified by re-designing it as "carry look ahead adder". Illustrate the functionality of it using two 4-bit numbers A=1101 and B=1011. (10)

4) What is the significance of a priority encoder? Explain the functionality of a 4:2 priority encoder. Write Verilog code for 8:3 priority encoder using casex statement. (10)

5) With neat circuit diagram along with truth table and transistor states, illustrate how to realize NAND, NOR and AND gates using a NMOS transistor. (10)