Exam Date & Time: 12-May-2023 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
END SEMESTER THEORY EXAMINATION - MAY 2023
II SEMESTER B.Sc (Applied Sciences) in Engg.

Switching Circuits and Logic Design [ICS 122 - S2]

Marks: 50 **Duration: 180 mins.**

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Answer all the questions.

Missing data, if any, may be suitably assumed

1) i) Simplify the following expression using consensus theorem

g(a,b,c,d)=a'c'd'+a'bd+bcd+acd'+b'cd'

ii) Express DeMorgan's theorem in terms of logic gates.

iii) Write the prime implicants, essential prime implicants and simplified expression for the following function. (10)

F(a, b, c, d)= ∑m(1, 3, 4, 5, 10, 11, 12, 13, 14, 15)

2) Define multiplexer and design the following multiplexers.

i) using 2-to-1 multiplexers to build a 4-to-1 multiplexer.
ii) using 4-to-1 multiplexers to build a 16-to-1 multiplexer. (10)

Write behavioural Verilog code for 3 to 8 decoders with active high enable input and active low output. Use case Statement.

3) Design a circuit for BCD adder using 4-bit binary adder and derive its SOP expression which is used as correction circuit. Explain its operation in detail. (10)

4) Design a circuit and write Verilog code for the following

i) 4-bit binary into equivalent grey code
ii) 4-bit grey code into equivalent binary (10)

5) With neat circuit diagram along with truth table and transistor states illustrate how to realize NOT, NAND and NOR gates using CMOS transistor. (10)

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