MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

II SEMESTER M.TECH. (INDUSTRIAL AUTOMATION & ROBOTICS)

End-semester Examination

SUBJECT: EMBEDDED SYSTEM FOR AUTOMATION (MTE 5251)

Date: 22/05/2023

Time: 3 Hours **Exam time: 9.30 AM– 12.30 PM** **MAX. MARKS: 50**

Instructions to Candidates:

- *Answer ALL the questions.*
- *Missing data may be suitably assumed and justified.*

Q. No.		M	CO/ CLO	PO/LO	BL
1(a)	Embedded systems are essential for controlling and monitoring a variety of machinery, equipment, and processes in industrial automation, which is crucial for enhancing manufacturing processes' productivity, effectiveness, and cost-effectiveness. Discuss the sustainable design of an embedded system utilized in industrial automation that can be estimated and enhanced	**4**	**1**	**4/7**	**5**
1 (b)	You are a product manager for a technology company, facing a challenging situation regarding launching a highly anticipated new product. Due to unforeseen delays in the market, your company is at risk of incurring significant losses. Your task is to analyze the situation by considering the simple revenue model and proposing strategies to mitigate the potential loss.	**4**	**1**	**4/2**	**4**
1 (c).	Develop an assembly language program to calculate the factorial of 7 for MSP432P401R and save the result into the memory location 0x20000000.	**2**	**1**	**4/1**	**3**
2 (a).	You have a robotic arm that needs to be controlled using a DC motor. The motor needs to be turned on and off every 1 second using a blue LED as an indicator. Write an embedded C program for MSP432P401R that uses the one-shot mode of Timer32 to toggle the blue LED every 1 second and control the DC motor accordingly. Consider the Mclock = 3MHz	**5**	**2**	**4/1**	**3**

2 (b).	A 3-stage pipelined CPU to run 3-iteration of the following code.
	
	MOV R1, #2
	L1 AND R2, R2, #1
	B L1
	MOV R3, #3
	MOV R4, #4
	(a). Determine the number of instruction cycles the CPU requires to execute the program with the help of a pipelining diagram.
	
	(b). Also, calculate the number of branch penalties.
		3	**2**	**4/2**	**4**

	<table><tr><td>Bits</td><td>7</td><td>6</td><td>5</td><td>3-2</td><td>1</td><td>0</td></tr><tr><td>TIMER32_y->CONTROL</td><td>ENABLE</td><td>MODE</td><td>IE</td><td>PRESCALE</td><td>SIZE</td><td>ONESHOT</td></tr><tr><td>TIMER32_CONTROL_XX_x</td><td>1-enable, 0-disable</td><td>0- free runnin g mode, 1- periodic</td><td>1- enable interr upt 0- disabl e</td><td>00=/1, 01=/16, 10=/256</td><td>1- 32 bit, 0- 16 bit</td><td>1-oneshot, 0-wrap</td></tr></table> <table><tr><td>25</td><td>Timer32_INT1</td><td>T32_INT1_IRQn</td><td>T32_INT1_IRQHandler</td></tr><tr><td>26</td><td>Timer32_INT2</td><td>T32_INT2_IRQn</td><td>T32_INT2_IRQHandler</td></tr></table> <table><tr><td>TIMER32_y->LOAD</td><td>Load register</td></tr><tr><td>TIMER32_y->INTCLR</td><td>Clear flag</td></tr><tr><td>TIMER32_y->VALUE</td><td>Check the counter value</td></tr></table>				
2(c)	Estimate the clock frequency and efficiency of the 5-stage pipeline. Assume the time delay of the circuit in each stage is 0.6micro second, the latch delay of 0.003 microseconds, and the total number of data that need to be processed is 30.	**2**	**2**	**4/1**	**3**
3(a)	You are designing a digital system for controlling the speed of a motor. In your design, you can use Complex Programmable Logic Devices (CPLDs) or Field-Programmable Gate Arrays (FPGAs). • Explain the differences between CPLDs and FPGAs regarding their architecture and functionality? • Comment on which would be best suited for this application.	**5**	**3**	**4/1**	**3**
3(b)	Assume the following processes arrive for execution at the indicated time and mention the tire CPU-burst time length given in milliseconds. <table><tr><th>Job</th><th>Burst time (ms)</th><th>Priority</th><th>Arrival time (ms)</th></tr><tr><td>A</td><td>10</td><td>5</td><td>0</td></tr><tr><td>B</td><td>6</td><td>2</td><td>0</td></tr><tr><td>C</td><td>7</td><td>4</td><td>1</td></tr><tr><td>D</td><td>4</td><td>1</td><td>1</td></tr><tr><td>E</td><td>5</td><td>3</td><td>2</td></tr></table> Calculate the average waiting and turnaround time for the pre-emptive priority scheduling algorithm	**3**	**3**	**4/1**	**3**
3(c)	Design a logic diagram of the following function using XOR and AND gates only. F = A. B'CD' + AB'CD' + A. B'C'D + A'BC'D	**2**	**3**	**4/2**	**4**
4(a)	As a manufacturing engineer, you are instructed to design a PCB for a high-speed digital system. Explain the characteristics of a PCB design in detail to ensure optimal performance and reliability of the digital system.	**3**	**4**	**4/1**	**3**
4(b)	In an embedded system, the Printed Circuit Board (PCB) plays a crucial role in determining the performance and reliability of the system. Examine the importance of PCB in embedded systems.	**3**	**4**	**4/2**	**4**
4(c)	Wireless networks have become increasingly vulnerable to security breaches, raising concerns about data privacy and confidentiality. Develop a digital circuit free from race-around conditions as a design engineer to create a secure communication channel within a wireless network application. Examine the digital circuit in detail with a proper circuit diagram and analysis.	**4**	**3**	**4/2**	**4**
5(a)	In the bottling industry, engineers are tasked to design an automation circuit using combinational logic with three sensors, S1, S2, and S3,	**6**	**3**	**4/3**	**5**

	detecting the bottles' height, width, and company logo, respectively, and two actuators, A1 and A2, directing the bottles to the defective or error/inspection lane based on the input from the sensors. The following conditions should be satisfied by the automation circuit: • If all the Sensors are off, the actuators A1 and A2 do not direct bottles to any of the lanes. • If S1 and S2 are off and S3 is on, the A2 will send the bottle to the error/inspection lane. • If S1 and S3 are off and S2 is on, the A2 will send the bottle to the error/inspection lane. • If S2 and S3 are on and S1 is off, the A1 will send the bottle to the defective lane. • If S2 and S3 are off and S1 is on, the A2 will send the bottle to the error/inspection lane. • If S1 and S3 are on and S2 is off, the A2 will send the bottle to the error/inspection lane. • If S1 and S2 are on and S3 is off, the A2 will send the bottle to the error/inspection lane. • If S1, S2, and S3 are on, then A1 and A2 are off and do nothing. From the above information, estimate the following parts. 1. Evaluate the truth table for the above logic. 2. Derive the Boolean expression for the combinational circuit. 3. Design the combinational circuit using logic gates.				
5(b)	Elaborate the Field-Programmable Gate Arrays (FPGAs) architecture. Also, briefly explain the working principle of Configurable Logic Blocks (CLBs) using a suitable diagram.	**4**	**3**	**4/1**	**3**