

Question Paper

Exam Date & Time: 29-May-2023 (10:00 AM - 01:00 PM)



MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
Second Semester Master of Engineering - ME (Embedded Systems) Degree Examination - May 2023

Digital Signal Processing [ESD 5001]

Marks: 100

Duration: 180 mins.

Monday, May 29, 2023

Answer all the questions.

- 1) Sketch Radix-2 DIF-FFT algorithm to find the DFT of the sequence $x(n) = [1, 1, 1, 0, 0, 1, 1, 1]$. (10)
Using this result obtain the DFT of the sequence $y(n) = [1, 1, 1, 1, 1, 0, 0, 1]$
- 2) Sketch the hardware for the following system function using Direct form-I, Direct form-II and Cascade form (10)
 $H(z) = [(1 - 0.25z^{-1})(z^2 - 5z^{-1} + 6)] / [(z^2 - 2z^{-1} + 2.5)(1 - 0.75z^{-1})]$
- 3) Demonstrate in detail the frequency sampling technique for the design of FIR filters (10)
- 4) It is desired to remove low frequencies in an analog signal with a digital linear phase FIR filter. The 3 dB frequency is 2 KHz, transition width is 500 Hz and the stop band attenuation is 50 dB. Design and Construct the hardware of the filter using suitable window function to meet the above specification. The filter employs a sampling frequency of 10 KHz (10)
- 5) Design and Construct the hardware using bilinear transformation technique, a digital Butterworth lowpass filter with the following specifications. (20)
 $|H(j\Omega)| \geq -1 \text{ dB } 0 \leq \Omega \leq 100 \text{ rad/sec}$
 $|H(j\Omega)| \leq -40 \text{ dB } \Omega \geq 2000 \text{ rad/sec.}$
Sampling frequency = 8000 rad/sec.
- 6) What is Multirate Signal Processing? Demonstrate the expressions both in time domain and frequency domain for the signal whose sampling rate is changed by a rational factor I/D (10)
- 7) What is a digital filter bank? Apply multirate signal processing to explain the implementation of uniform DFT filter bank (10)
- 8) Explain analytically, how optimum filter coefficients are obtained on Mean Square Error sense in Wiener Predictor Configuration (10)
- 9) Explain the TMS320C6X DSP processor pipelining operation (10)

-----End-----