Question Paper

Exam Date & Time: 28-Jun-2023 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
Second Semester Master of Engineering - ME (VLSI Design) Degree Makeup Examination - June 2023

Advanced VLSI Design [VLS 5201]

Marks: 100 **Duration: 180 mins.**

Wednesday, June 28, 2023

Answer all the questions.

1)	a) Explain the effect of Temperature and Voltage on CMOS Resistor. b) Estimate the minimum and maximum resistance of an n-well resistor with a length of 100µm and a width of 10µm over a temperature range of 0 to 100°C. [Data Given: TCR = 10,000ppm/°C; N-well sheet resistance = 2KΩ to 3KΩ/square]	(10)
2)	Write a note on different SPICE and BSIM MOSFET models. Explain a few important parameters used by them.	(10)
3)	Draw and explain the circuit of Cascode current mirror and show that output resistance of the n-stage cascode current mirror $R_{o(n)} = r_o(1+g_mR_{o(n-1)}) + R_{o(n-1)}$, where r_o is output resistance of all the MOSFETs, gm is the transconductance of all the MOS used in the circuit.	(10)
4)	With a diagram, explain cascode current mirror. List its advantages over a simple current mirror?	(10)
5)	Show how can we maximize the voltage gain of a CMOS Common-Source amplifier with passive resistor load? Illustrate the different trade-offs that should be done. Obtain the expression for the gain considering channel-length modulation.	(10)
6)	With the help of a small-signal equivalent circuit, develop an expression for A_v for a CMOS Common-Gate amplifier with passive resistor load. Assume finite output impedance, r_0 and signal source impedance r_s.	(10)
7)	Describe a ***Common Mode Range*** (CMR) of a differential amplifier? Explain, with diagram, how do you measure it?	(10)
8)	Explain ***charge injection*** and ***clock feedthrough*** in a MOSFET switch? Discuss a method used to reduce their effect.	(10)
9)	Discuss the different errors that occur in a *Sample-and-Hold* circuit.	(10)
10)	Develop expressions for $\|INL\|_{max}$ and $\|DNL\|_{max}$ for a simple Resistor string DAC.	(10)

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