Question Paper

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
Second Semester Master of Engineering - ME (VLSI Design) Degree Examination - May 2023

Low Power VLSI Design [VLS 5202]

Marks: 100   **Duration: 180 mins.**

Friday, 26 May, 2023

Answer all the questions.

1)   Derive an expression for the short-circuit power dissipation component in a CMOS circuit. Discuss how   (10)
            to reduce short-circuit power.

2)   Explain, with the help of a diagram, how a natural stacking of transistors controls the sub-threshold   (10)
            leakage current.

3)   Discuss the following multiple V_{th} techniques :   (10)
            a) Multi-threshold CMOS (MTCMOS) (5)
            b) Dual Threshold CMOS (5)

4)   The following circuit is implemented in 65 nm CMOS technology, which suffers from high leakage. For high speed, only   (10)
     low threshold transistors have been used. Each gate has a delay of 5ps and a leakage current of 10nA.
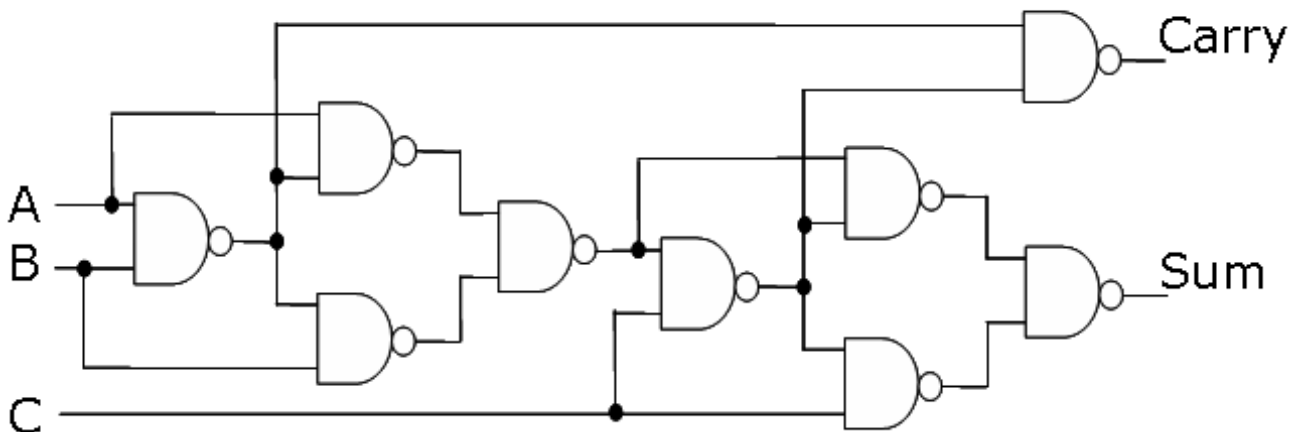
a) Given that a gate with high threshold transistors has a delay of 12ps and leakage of 1nA, optimally assign thresholds
to gates to minimize the leakage current without increasing the critical path delay for Carry output. Assume that delay of
Sum output is not critical. What is the percentage reduction in leakage power?
b) Is it possible to further reduce leakage by redesigning the circuit? If yes, show how much reduction you can obtain.
c) Are the dual threshold designs better or worse than the all low threshold design for glitch power?

5)   Describe the Reliability-Driven Voltage Scaling approach for dynamic power reduction.   (10)

6)   Discuss the Architecture-Driven Voltage Scaling technique by trading area for lower dynamic power   (10)
            through hardware duplication.

7)   Explain Gate Triggering Approach to minimize the glitch power with an example.   (10)

8)   Illustrate and explain the principle of operation of Adiabatic Power Supply.   (10)

9)   Discuss the basics of modeling power in current EDA tools. Explain Scalable Polynomial Power Models.   (10)

10)   Describe the timing issues in multi-voltage designs.   (10)

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