# Question Paper

Exam Date & Time: 22-May-2023 (10:00 AM - 01:00 PM)

## MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
Second Semester Master of Engineering - ME (VLSI Design) Degree Examination - May 2023

**Physical Design Elective -2 [VLS 5234]**

**Marks: 100** **Duration: 180 mins.**

**Monday, May 22, 2023**

**Answer all the questions.**

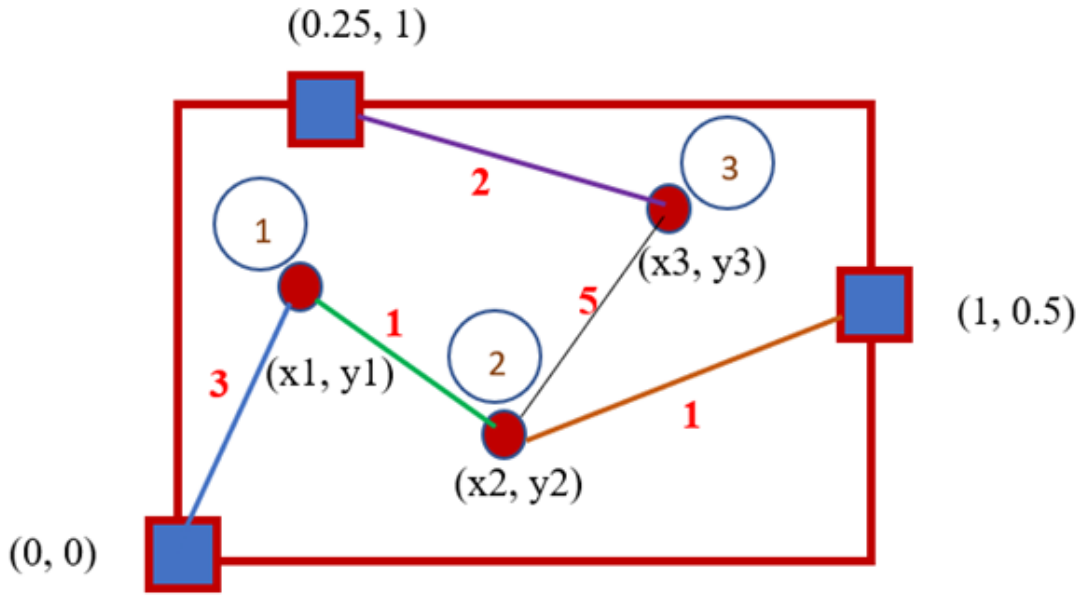
1) List and explain the properties of static CMOS and dynamic CMOS logic gates (10)

2) Describe any three layout design rules and implement the function f=! (ab+cd) in static CMOS logic and draw the stick diagram for the same (10)

3) List the data required for floorplan. Explain the technology and library files with suitable examples. (10)

4) Explain IO pad placement and power planning in physical design step (10)

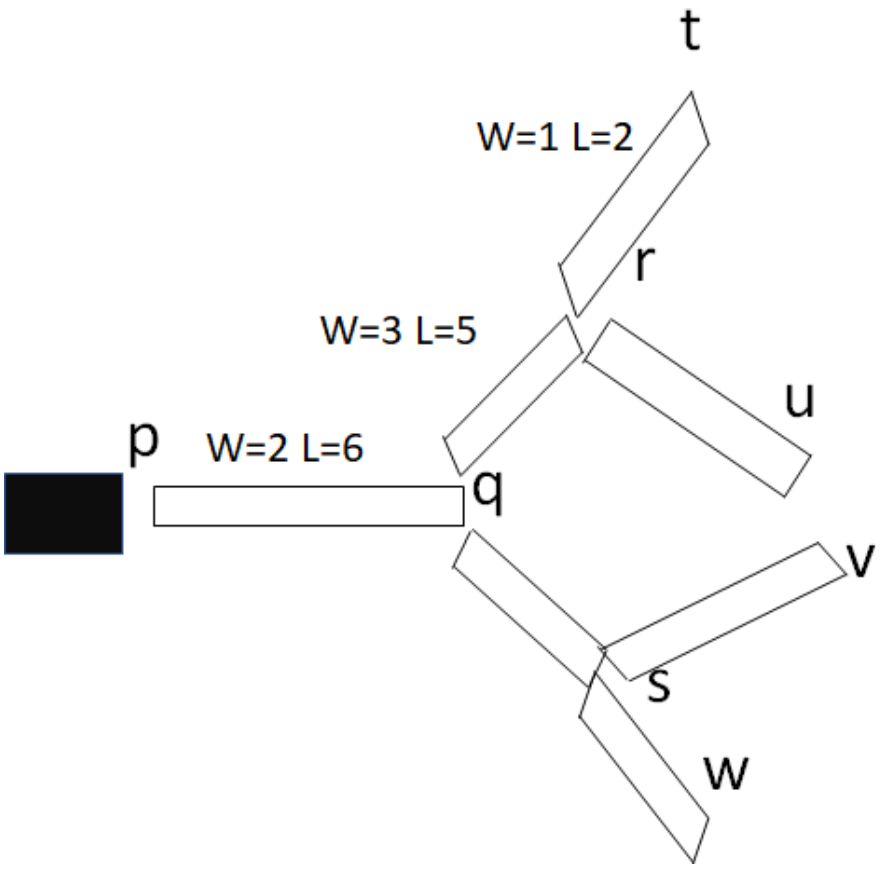
5) Compute and draw the locations of gates 1, 2, and 3 shown below using quadratic analytical placement (10)




6) Apply and explain maze routing steps of global routing with multi targets and multi metal layers with examples (10)

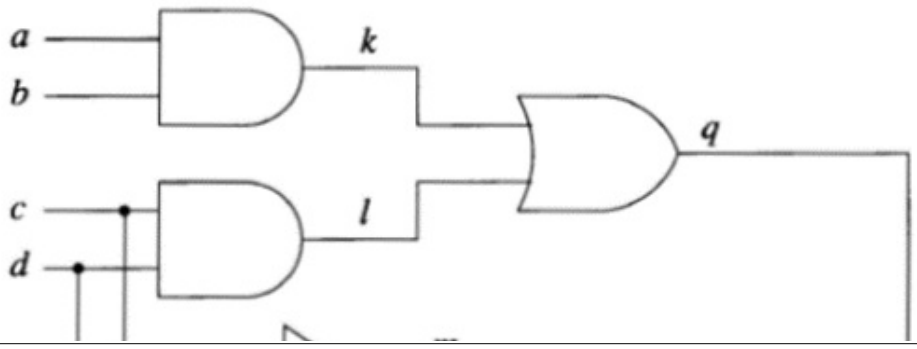
7) Calculate delay at output nodes t and v. Assume a capacitance of 2 units at each output. (10)
Consider R=r*L /W and C=c*W*L , assume r=1.5 and c=3

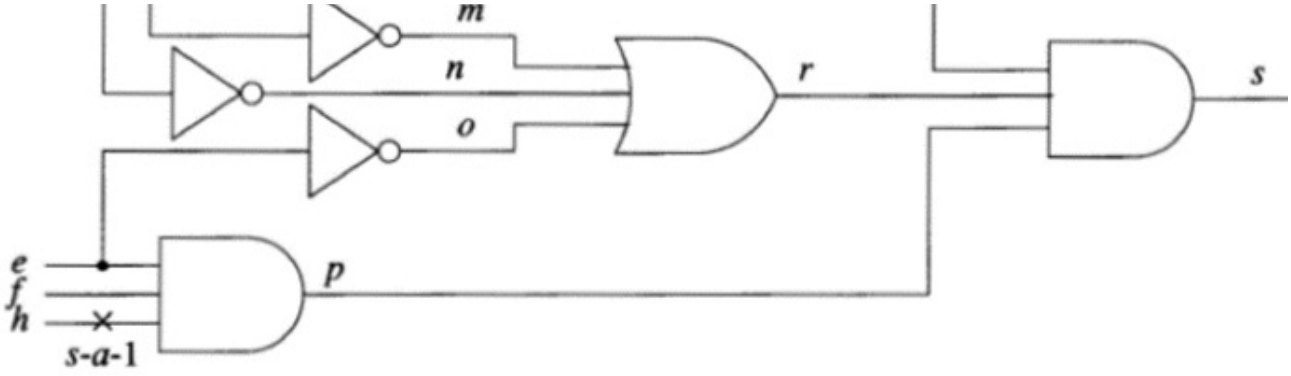
Consider R=F L/W and C=ε W L, assume f=1.5 and ε=5




8) Compute the collapse ratio for a carry circuit of a 1-bit full adder gate level circuit. (10)

9) Identify and explain the test vector for s-a-1 fault at h (10)






10) Define Built in Self Testing (BIST). How a pseudo random pattern can be generated using linear feedback shift registers. Explain with the help of an example. (10)

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