Question Paper

Exam Date & Time: 31-May-2023 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
Second Semester Master of Engineering - ME (VLSI Design) Degree Examination - May 2023

Universal Verification Methodology [VLS 5204]

Marks: 100 **Duration: 180 mins.**

Wednesday, May 31, 2023

Answer all the questions.

1)	Describe shallow copy and deep copy methods in Object Oriented Programming with suitable program and mention the sample output	(10)
2)	Outline the UVM class library hierarchy. Describe UVM component utility with an example	(10)
3)	Describe uvm_sequence_item class in UVM. Provide a program to describe sequence_item copy and sequence_item clone	(10)
4)	Describe driver class in UVM component with the help of a program	(10)
5)	Explain the uvm_sequence class in UVM with the help of a program	(10)
6)	Describe the uvm report in UVM with the help of a program	(10)
7)	Explain overriding in UVM. Provide an example for overriding by type and parameterized type	(10)
8)	List any five advantages of register abstraction layer. Explain uvm_reg_block and uvm_reg_file	(10)
9)	Describe set & get, update, mirror, randomize, and reset methods in register abstraction layer	(10)
10)	Explain TLM blocking get_port with the help of a UVM program	(10)

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