Question Paper

Exam Date & Time: 15-Jan-2024 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

3rd SEM B. Tech (BME) DEGREE
END SEMESTER MAKE-UP EXAMINATIONS, JAN-2024
SUBJECT: DIGITAL SYSTEM DESIGN (BME 2123)

DIGITAL SYSTEM DESIGN [BME 2123]

Marks: 50 **Duration: 180 mins.**

Descriptive

Answer all the questions.

1A) Illustrate the following using Active high and Active low decoder F(A,B,C) =∑m(1,2,3,4) and G(A,B,C) = ∑m(0,2,6,7) (5)

1B) Design a half subtractor using NOR gate only (3)

1C) Write the a) Standard POS and b) Minimized POS for the given Truth Table (2)

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	1

2A) Design the minimum CMOS transistor network that implements the functionality of Boolean equation
F= (A (B C + D))' (4)

2B) Design a 2:1 MUX with the help of neat circuit and corresponding truth table considering the details of pull up and pull down transistors (4)

2C) Implement the given Boolean function using CMOS TX gate (2)

F= AB + AC + CD

3A) Solve the following function using PAL (5)

A (x,y,z) = ∑ m (1,2,4,6)

B (x,y,z) = ∑ m (0,1,6,7)

C (x,y,z) = ∑ m (2,6)

D (x,y,z) = ∑ m (1,2,3,5,7)

3B) Solve the following function using PLA (3)

F1= ∑ m (3,5,7) and F2 = ∑ m (4,5,7)

3C) Generalize any two differences between CPLD and FPGA (2)

4A) Illustrate S-R Flip flop with all cases using NAND gates with relevant logic diagram and Truth table (4)

4B)	Explain with a neat diagram the structure of CPLD.	(4)
4C)	Explain D flip flop with relevant block diagram and Truth table.	(2)
5A)	Design CMOS SR Latch using NAND gates with a) Circuit diagram of SR Latch b) Truth table of SR Latch c) Pull up and pull down circuit	(5)
5B)	Write a short note on standard cells	(3)
5C)	Design a two input NMOS NOR gate with the help of neat circuit and corresponding truth table	(2)

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