Question Paper

Exam Date & Time: 08-Jan-2024 (09:30 AM - 12:30 PM)



MANIPAL ACADEMY OF HIGHER EDUCATION

THIRD SEMESTER B.TECH END SEMESTER MAKEUP EXAMINATIONS, JAN 2024

ELECTRONICS CIRCUITS [BME 2122]

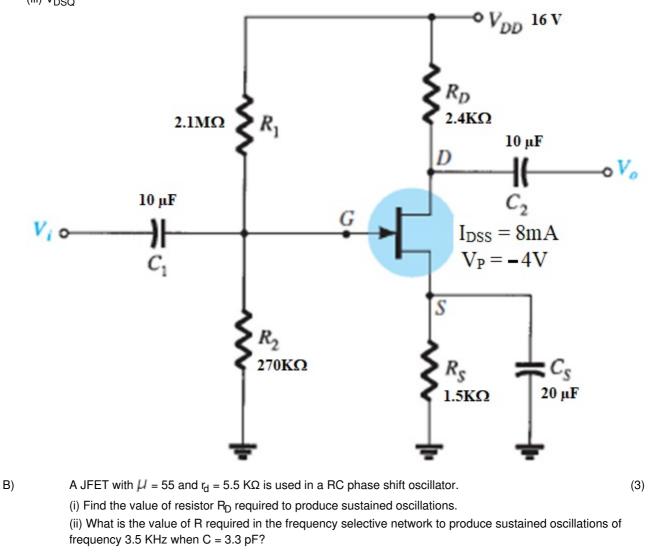
Marks: 50

Answer all the questions.

Missing data may be suitably assumed Draw neat circuit diagrams wherever necessary

- For the JFET amplifier circuit shown below, using graphical solution determine

 I_{DO}
 - A) (ii) V_{GSQ}, and (iii) V_{DSQ}



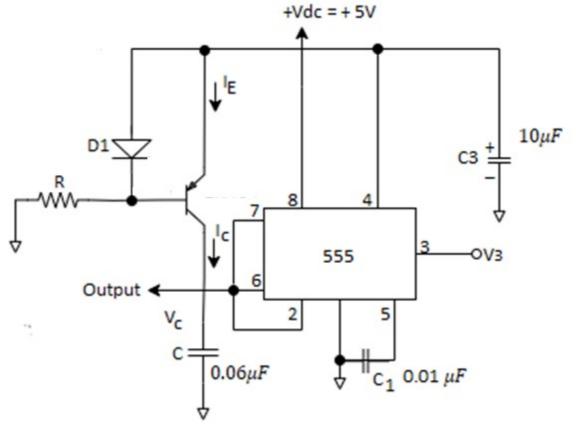
C) Design an Op-amp non-inverting amplifier such that the amplifier develops an output of 0.1V when the (3) input is 1mV. Depict the designed amplifier circuit.

(4)

Duration: 180 mins.

2)	Develop an Op-amp based astable multivibrator circuit to produce an output of frequency 1 KHz with 50% duty cycle and amplitude \pm 14V.	(4)
A)		
B)	How do you make use of an Op-amp as an inverting adder? Explain with an example.	(3)
C)	Design an inverting Schmitt trigger circuit using an Op-amp such that $V_h = 7V$ and maximum output swing is \pm 14V.	(3)
3)	Build a 3-bit ADC using the following: (i) Resistive voltage divider network	(4)

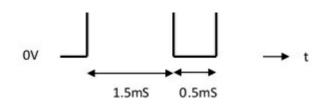
- A) (ii) Op-Amps, and
- (iii) Priority encoder
- B) What is the resolution and full-scale output of an 8-bit R-2R Ladder digital-to-analog converter, when (3) $V_{REF} = 10V$ and $R_F = 2R$?
- C) In the following circuit, what is the value of R required to generate a free-running ramp of frequency 1 KHz? (3) Assume that the diode and transistors are made up of Silicon.



4)	How do you build a constant current source using voltage regulator IC 7805? Explain in detail.	(5)
A)		
B)	How do you make use of a 555 timer as a Schmitt trigger? Explain in detail.	(3)
C)	Using a 7805 voltage regulator IC, design a 600 mA current source. Assume a quiescent current of 4.0 mA.	(2)
5)	Design a 555 timer based circuit to generate a periodic waveform as shown below.	(4)

A)

5V



- B) How do you make use of 555 timer IC to build a negative edge mono-shot circuit? Explain, and derive an (4) expression for the pulse width.
- C) If a p-channel JFET has $I_{DSS} = 8mA$ and $V_{GS(off)} = 6V$, what is the value of Gate-to-source voltage (2) required to produce a drain current of 4 mA and what is the magnitude of pinch-off voltage?

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