Question Paper

Exam Date & Time: 05-Jan-2024 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

THIRD SEMESTER B.TECH. EXAMINATIONS - JANUARY 2024
SUBJECT: CSE 2121- COMPUTER ORGANIZATION & ARCHITECTURE

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

1A)	Consider that a list of 32-bit positive integers are stored in the memory from the location named LIST. The word at address ELE is to hold the value of the smallest number after it has been found in this list. Assuming, the number of entries in the list is present at the memory location N, Write a RISC-style program to find the smallest number in the list.	(5)
1B)	Convert the following pairs of decimal numbers to 6-bit 2's-complement numbers and perform the operation mentioned. State whether overflow occurs or not in each case. Also, if overflow has occurred, state why it has occurred. i) Add 4 and 11 ii) Subtract –9 from -2	(2)
1C)	Perform floating point multiplication of the following numbers and represent the result in IEEE 32 bit format. X= 3.344 * 10^1 and Y= 8.877 * 10^-2	(3)
2A)	Apply the Non-Restoring division algorithm to perform the following division 14/3	(3)
2B)	Express the following number in IEEE 32-bit floating-point format. (i) 1/16	(2)
2C)	Consider the state diagram given below in figure 2C. Based on the below diagram perform the following: i) Draw the block diagram of the controller ii) Draw the logic diagram of the controller indicating appropriate counter, decoder and sequence controller iii) Derive the truth table of the sequence controller and provide expressions for the output terms of the sequence controller iv) Implement the sequence controller with the PLA .	(5)

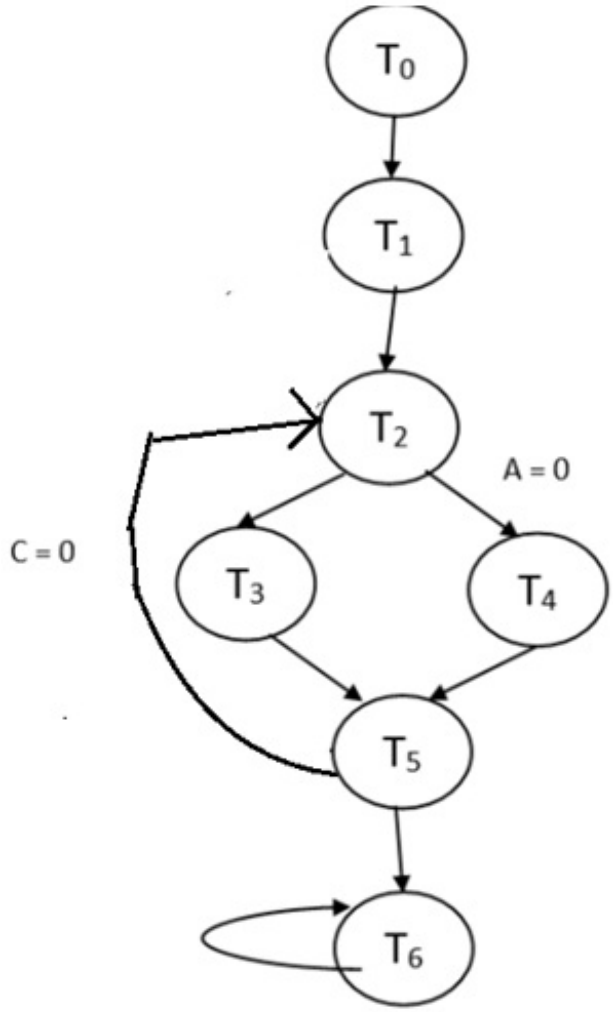

Fig. No 2C

3A)	Draw neat diagrams of one bus and three bus architectures. Analyse the number of clock cycles to $R2 \leftarrow R0+R1$, assuming that the source and destination are the general-purpose registers.	(3)
3B)	Design a 2G×32 memory module using 256×8 static memory chips. Draw a neat diagram indicating address lines, data lines and explain its working.	(5)
3C)	Consider a 4-way set associative mapped cache of size 32 KB with block size 256 bytes. The size of main memory is 128 MB. Find the size of tag, set and word fields.	(2)
4A)	Explain how write-buffers enhance cache accesses in the case of write-through and write-back protocols.	(3)
4B)	Explain disk controller and its functions. Consider a disk that has an average seek time of 32ns and a rational rate of 360rpm. Each track of the disk has 512 sectors and each sector has a size of 512 bytes. What is the time taken to read four continuous sectors? Also, determine the data transfer rate.	(5)
4C)	How are interrupts from multiple devices handled through vectored interrupts?	(2)
5A)	What is the need for cache coherence in a shared-memory multiprocessor architecture? Explain how Write-back protocol ensures cache coherence.	(5)
5B)	Briefly explain how processor and GPU co-ordinate execution of instructions in a computing system.	(3)
5C)	Compare and contrast Memory-mapped I/O and I/O mapped I/O addressing techniques	(2)

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