Question Paper

Exam Date & Time: 30-Nov-2023 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

THIRD SEMESTER B.TECH. EXAMINATIONS - NOVEMBER / DECEMBER 2023
SUBJECT: CSE 2121- COMPUTER ORGANIZATION & ARCHITECTURE

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

1A)	Assume that a list of non-repetitive integers is present in a byte-addressable memory starting from the location 1000 and the number of elements in this list is present at the location N. Using Indexed Addressing Mode, write a RISC style program that searches for an element in this list of numbers. Let the search element be available at location NUM. If it occurs in the list, then a separate memory location named ELE must be updated with effective address where the element was found, else 0.	(5)
1B)	Add the following pairs of decimal numbers after representing them in 5-bit 2's complement format. Check and justify if overflow occur in each case. i) 7 and 15 ii) -5 and 9	(2)
1C)	Using the Restoring Division algorithm, divide the following: divisor= 4 and dividend= 7.	(3)
2A)	Perform the Booth's multiplication of the following numbers after representing them in 7-bit 2's complement format: M=33 and Q= -23	(3)
2B)	State the arithmetic addition and subtraction rules of signed integers.	(2)
2C)	Provide the binary listing of microprogram for the Register Transfer Description given below. Show all the necessary steps to arrive at the binary listing.	(5)

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Declare registers A[8], B[8]
Declare inbus[8], outbus[8]
START:   A←inbus
         B←inbus
BACK:    If B <> 0 then go to ADD
         go to SUB
ADD:     A←A+B
         go to NEXT
SUB:     A←A-B
NEXT:    B←B-1
         If A = 0 then go to BACK
         outbus = B
HALT:    go to HALT
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3A)	Draw neat diagrams of Two-Bus and Three-Bus architectures. Explain how many clock cycles are required in each to perform addition operation assuming that the source and destination are general purpose registers.	(3)
3B)	Design a byte-addressable memory module of size 1K x 8 using bit cells with a neat diagram. Calculate the number of address lines and data lines in the final design.	(5)
3C)	Consider a computer that has the following parameters. Access times to the cache and the main memory are 4τ and 40τ, respectively. When a cache miss occurs, a block of 16 words is transferred from the main memory to the cache. It takes 40τ to transfer the first word of the block, and the remaining words are transferred at the rate of one word every 4τ seconds. Assume that 30 percent of the instructions in a typical program perform a Read or a Write operation, which means that there are 130 memory accesses for every 100 instructions executed. Assume that the hit rates in the cache are 0.95 for instructions and 0.9 for data. Assume further that the miss penalty is the same for both read and write accesses. Compute the access time with cache.	(2)
4A)	Illustrate with the diagram on how disk controller is connected with the system bus in detail. Consider a disk unit has 22 recording surfaces. It has a total of 12,300 cylinders. There is an average of 320 sectors per track. Each sector contains 512 bytes of data. i) What is the maximum number of bytes that can be stored in this unit? ii) What is the data transfer rate in bytes per second at a rotational speed of 6400 rpm?	(3)
4B)	Consider a block set-associative cache. It consists of 64 blocks divided into 4 block sets. The main memory contains 4096 blocks, each consists of 128 words of 16 bits length. Depict the organization of the cache through a neat diagram. i) How many bits are there in main memory? ii) How many bits are there in each of the TAG, SET and WORD fields?	(5)
4C)	Indicate how the process and threads are differentiated? Explain Coarse-grained and Fine-grained multi-threading.	(2)
5A)	Explain the concept how DMA data transfer happens between various I/O devices and memory. Also, elaborate on the role of processor, DMA controller in this transfer operation with the help of a suitable diagram.	(5)
5B)	Consider the shared memory multiprocessor model used in the advanced computation system. Compare UMA and Non-UMA methods. Justify how these methods impact the performance of the computation with the necessary diagrams.	(3)
5C)	Why is Pipelining widely used in modern computers? Draw the block diagram showing the organization of a pipeline with five stages.	(2)

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