Question Paper

Exam Date & Time: 12-Jan-2024 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

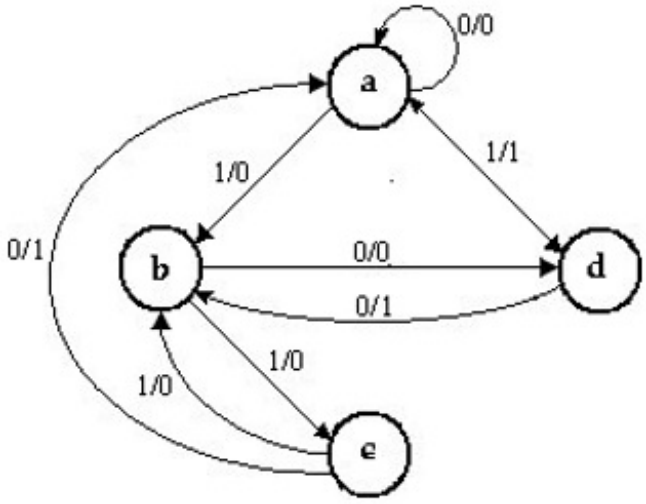
THIRD SEMESTER B.TECH. DEGREE EXAMINATIONS -JANUARY 2024
SUBJECT: CSE 2123- DIGITAL SYSTEM DESIGN

Marks: 50 **Duration: 180 mins.**

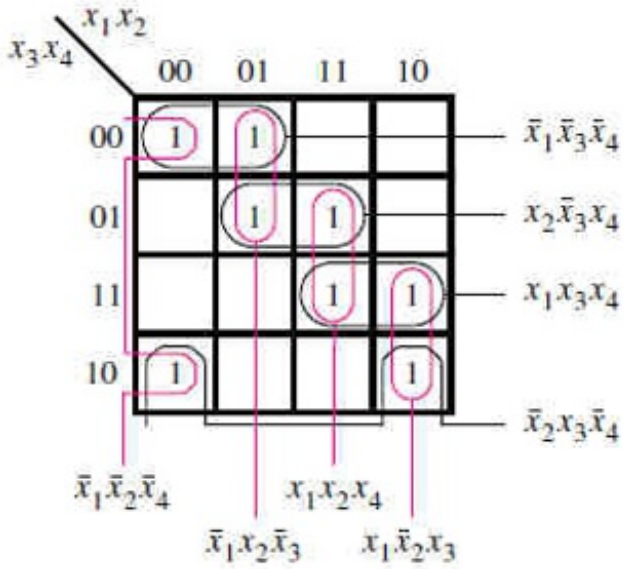
Answer all the questions.

Missing data may be suitably assumed.

1A) For the following state diagram, derive the expressions required for the synchronous sequential circuit design using T flip-flops. (5)



1B) Find the POS implementation for the following and compare the cost with the SOP form. (3)



1C) Explain in detail the design of a basic RS latch using NOR gates. (2)

2A) Design a control unit of a simple processor to perform the operations mentioned in Table below. For the control unit, (5)

a) Develop the timing signals for the operations
b) Tabulate the necessary control signals that needs to be asserted during the timings of a)
c) Derive the expressions for all the control signals of b).

Operation	Function
I0: Load Rx, Data	Rx ← Data
I1: Move Rx, Ry	Rx ← [Ry]
I2: Swap Rx, Ry	Rx ←→Ry
I3: Add Rx, Ry	Rx ← Rx + Ry
I4: Sub Rx, Ry	Rx ← Rx – Ry

Where,

a) Rx and Ry are the registers from R0, R1, R2, R3. All these registers are connected to a common bus through a tri-state buffer.
b) External data can be loaded into these registers with a tri-state buffer.
c) Use accumulator (A) and base register (B) for temporary operations with Arithmetic unit.
d) Each operation begins upon the assertion of signal W to 1
e) Completion of each operation is indicated by asserting the signal Done = 1
f) Use control signal $Add/\overline{Sub}$ to control the addition and subtraction operations.

2B) Implement the function $f(w_1, w_2, w_3) = \sum_m(1, 2, 3, 5, 6)$ can be formulated using a (3)

3-to-8 decoder and an OR gate.

2C) Explain how the restriction on the pulse width in the case of JK flip-flop can be solved by using master/slave JK flip-flop. (2)

3A) Design the synchronous counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6. Use JK flip-flops. Check if it is self-correcting or not. (5)

3B) Analyze the following state table and perform the state reduction. Develop the state diagram for the reduced state table. (3)

Present state	Next state		Output	
	x=0	x=1	x=0	x=1
a	a	b	0	0
b	c	h	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1
h	e	d	0	1

3C) Develop a state diagram for the FSM that meets the following specification: (2)
The circuit has one input, *w*, and one output, *z*. The output *z* should be equal to 1 in the same clock cycle when the second occurrence of *w* = 1 is detected. Otherwise, the value of *z* is equal to 0.
What is the output *z* produced for the following input sequence?
w: 1 0 0 1 1 1 1 0 0 1 1

4A) Develop the ASM chart for the bit counting circuit which counts the number of 1's in a register. Explain the same. Justify how it is different from traditional flowchart. (5)

4B) Construct a Johnson counter which generates 8 timing signals. Write the count sequence and AND gate expressions required for decoding the output. (3)

4C)	Construct CMOS NOR gate. Write the truth table and transistor states.	(2)
5A)	Build the D-type positive edge-triggered Flip-flop using NAND gates. Explain its operation with the logic diagrams for all the cases of D when the clock is low. Also, predict the outputs of the flip-flop for each case assuming that the flip-flop is cleared previously.	(4)
5B)	Design a hierarchical 40-bit carry look-ahead adder with ripple-carry between 8-bit blocks. Compute the total gate delay for the design mentioning all the intermediary gate delays.	(4)
5C)	Construct a 5-bit ring counter using D flip-flops.	(2)

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