Question Paper

Exam Date & Time: 07-Dec-2023 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

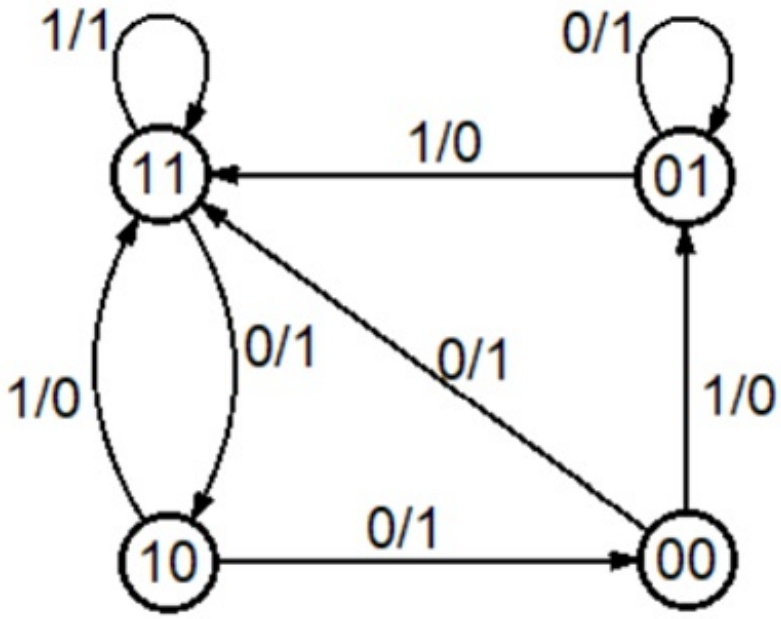
THIRD SEMESTER B.TECH. DEGREE EXAMINATIONS - NOVEMBER / DECEMBER 2023
SUBJECT: CSE 2123- DIGITAL SYSTEM DESIGN

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

Missing data may be suitably assumed.

1A) For the following state diagram, derive the expressions required for the synchronous sequential circuit design using JK flip-flops. (5)



1B) Make use of functional decomposition to find the minimum-cost circuit for the function $f(x1, x2, x3, x4) = \sum m(4, 7, 9, 10, 12, 13, 14, 15)$. Assume that the input variables are available in uncomplemented form only. (3)

1C) Demonstrate SR latch (basic Flip Flop circuit) using NAND gates with its function table. (2)

2A) It is required to develop a system to swap the contents of two n-bit registers. Assume that a temporary register is available to assist swapping. Adopt state table approach to design control circuit. Control circuit has two inputs clock and w. The swapping process is initiated when w=1, and on completion the control circuit asserts a signal Done to 1. (5)
i) Derive the expression for the outputs of control circuit.
ii) Develop bus architecture of the system based on tri-state buffer.

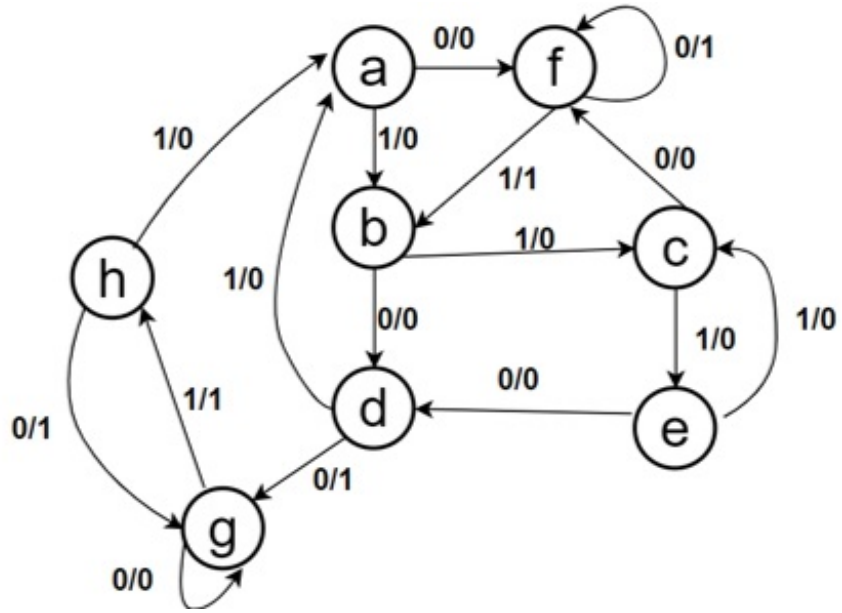
2B) A combinational circuit receives two single-bit inputs A and B and produces a single-bit output Y = F1|F2. The Boolean functions F1 and F2 are as given below and are implemented using a decoder and OR gates. Design a minimal circuit for Y using only one decoder, one 2:1 multiplexer, and OR gates. (3)
F1(A, B) = ∑m (2, 3)

F2(A, B) = ∑m (0,1,3)

2C) Construct JK Flip Flop from D Flip Flop (2)

3A) Design the synchronous counter with the following repeated binary sequence: 0, 1, 2, 4, 6. Use D flip-flops. Check if it is self-correcting or not. (5)

3B) Analyze the following state diagram and perform the state reduction. (3)



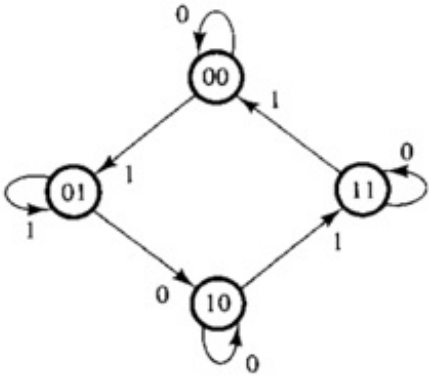
3C) Distinguish between Moore and Mealy models of sequential circuit design. (2)

4A) Since a computer has many registers, paths must be provided to transfer information from one register to another. An efficient scheme for transferring the information between registers in a multiple-register configuration is a common bus system. Design a 4-bit common bus system for 4-registers of 4-bits each using multiplexers. (5)

4B) Design 3-bit Johnson counter by implementing the following steps. (3)
a) Draw the state-transition diagram.
b) Construct state table using T flip-flops.
c) Design the Counter.

4C) Design NAND gate using CMOS technology. (2)

5A) Draw the state table and design the synchronous sequential circuit for the following state diagram using JK FF: (4)



5B) Design a combinational unit that can act as adder and subtractor for two 4-bit numbers. Provide suitable explanation. (4)

5C) Design a 4-bit ring counter using D flip-flops. (2)

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