Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, DECEMBER 2023

DIGITAL SYSTEM DESIGN [ELE 2122]

REVISED CREDIT SYSTEM

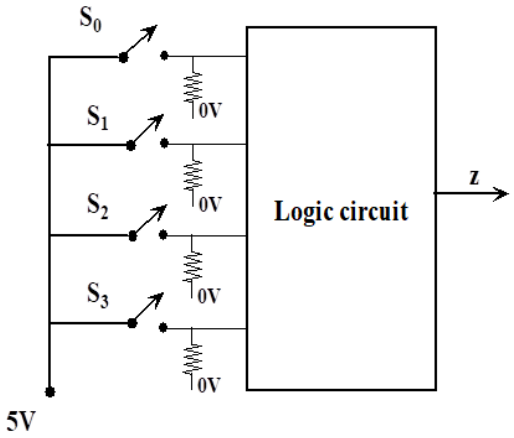
Time: 3 Hours **Date: 12 DECEMBER 2023** **Max. Marks: 50**

Instructions to Candidates:

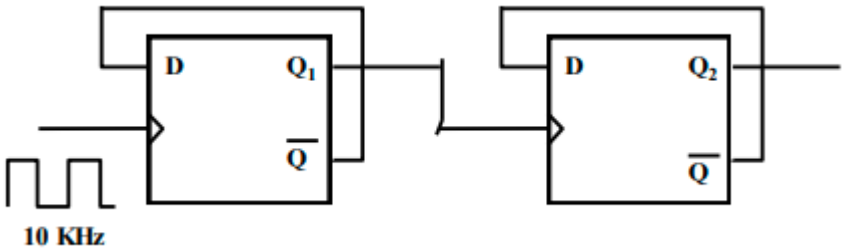
- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A	Apply VEM technique to obtain minimal SOP form of the given expression, F(a,b,c,d,e)= ∑(8,12,15,19,22,23,28,29,31)+d(0,1,4,7,13,16,24). Consider e as the MEV.	4
1B	The owner of a shopping complex wants an automatic sliding door at the shopping complex entrance with the following functional specifications. If a person is detected in front of the sliding door, the door should open else to be closed. However, there should be a provision for keeping the door manually open even if people are not at the door. Also, the shopping complex owner wants additional input for forcing the sliding door to be closed (even in the case of people at the door). Design a multiplexer-based digital system to control the sliding door satisfying the above conditions. Mention the required inputs and outputs. Develop the digital circuit using 2:1 multiplexer (you are allowed to take multiple multiplexers) and not gates.	3
1C	Design and develop a digital circuit of an even parity generator for 3-bit data sequence using 2 to 4 decoders and residual gates	3
2A	Design a Verilog HDL module for a system that controls two lights, M1 and L1, based on three binary sensors, S1, S2, and S3. Assume that the sensors can detect the presence or absence of a certain condition. M1 should be activated if either S1 or S2 is active, and L1 should be activated if S3 is active. Develop a Verilog HDL code considering the described control logic and declare appropriate input and output wires. (Use any modelling styles)	3

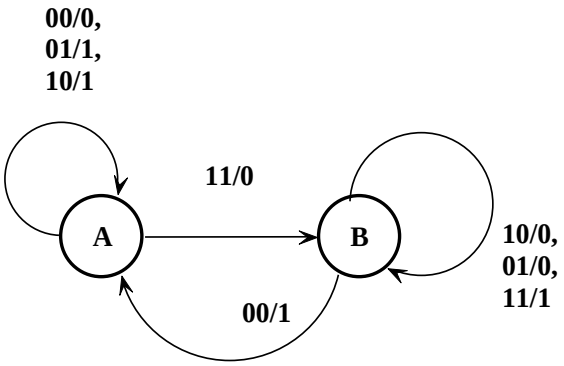
2B In a Xerox machine, the switches are present at various points along the path of the paper as the paper passes through the machine. The control circuitry of the machine is shown in the Figure. Each switch is normally open, and as the paper passes over a switch, the switch closes. The output of the logic circuit goes high whenever three or more switches are closed at the same time. Construct the truth table (min-terms) for the given functionality. Minimize the logic function using Tabulation method (Quine-McCluskey). 4



2C Develop the structural Verilog code for the circuit given below, by considering appropriate component as the instance. Analyze the circuit for its functionality. 3



3A Design the digital system represented by state diagram shown in the figure using D flipflops and residual gates. Use minimum number of gates and memory elements. 3



3B Formulate the Moore state diagram to detect 100 sequence, in a continuous data stream (Overlapping is allowed). Hence, write the Verilog HDL code for the same. 3

3C Design a 4- bit Johnson counter 4
a) Using behavioral Verilog HDL modeling style
b) Using Universal shift register IC 74LS194 (universal shift register)

4A Design a mod 9 up counter 3
a)using IC 7490 (mod 10 counter).
b)using Verilog HDL code

4B Alissa arrives home, but her keypad lock has been rewired and the old code number no longer works. A piece of paper is taped to it, showing the equation of the FSM-based door locking circuit implemented with D flip flops. The equations of the FSM are: 5

keypad lock (Z) = $Q_1.Q_2.x$,

$$D_1 = Q_1\bar{Q}_2x + \bar{Q}_1Q_2\bar{x}$$

$D_2 = x$

Where D_1 and D_2 are the flip flop inputs, x is the external input, z is the external output, Q_1 and Q_2 are the flip flop states. Develop the state diagram and Verilog HDL code for describing the circuit.

4C Determine the resulting value of Y in the expression, 2

Y = D + ~ B & C >> 3 ; using Verilog HDL operator concept.

Assume B= 4'b1000; C=4'b1111; D =4'b0010;

5A You are required to design a finite state machine (controller) of a coffee vending machine. The vending machine has a coin detector and it can detect the coins Rupees 5 and Rupees 10. The cost of the coffee is Rupees 8. The change return mechanism of the vending machine can return the changes in terms of Rs 1. Suggest a suitable finite state machine for the coffee vending machine with justification. Also, develop the state diagram for the same. 3

5B Construct the logic, **F = A'**, using CMOS logic families. Use minimum number of transistors. Write the Verilog HDL code for the same, using switch level modeling style. 3

5C Utilize Verilog HDL to design a dataflow model for a 2:1 multiplexer circuit. Treating mux(M) as a 2 to 1 multiplexer component, construct a structural Verilog HDL model to represent the following logic diagram. 4