Question Paper

Exam Date & Time: 05-Dec-2023 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

THIRD SEMESTER B.TECH. DEGREE EXAMINATIONS - NOVEMBER / DECEMBER 2023
SUBJECT: ECE 2121- ANALOG ELECTRONIC CIRCUITS

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

Missing data may be suitably assumed.

1A) The circuit shown in FIG.Q(1A) must be designed for a voltage drop of 200 mV across R_S. Assume $\mu_n C_{ox} = 200\mu A/V^2$ and $V_{TH} = 0.4V$. (4)
i) Calculate the minimum allowable value of (W/L) if 'M1' must remain in saturation.
ii) What are the required values of 'R_1' and 'R_2' for an input impedance of at least 30 KΩ?

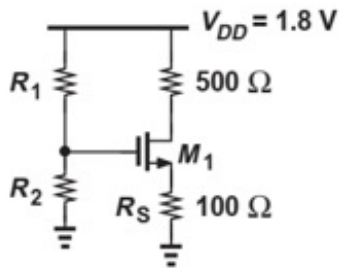

FIG.Q(1A)

1B) Draw the small signal model and determine the input impedance of the circuit shown in FIG.Q(1B). Assume λ = 0. (3)

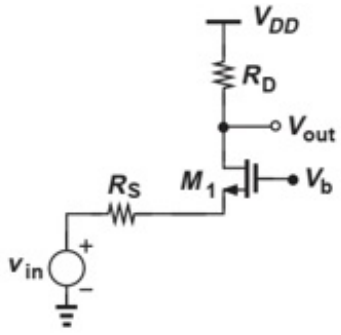

FIG.Q(1B)

1C) An integrated circuit employs the source follower and the common-source stage as shown in FIG.Q(1C). Design a current mirror that produces I_1 and I_2 from a 0.3 mA reference. (3)

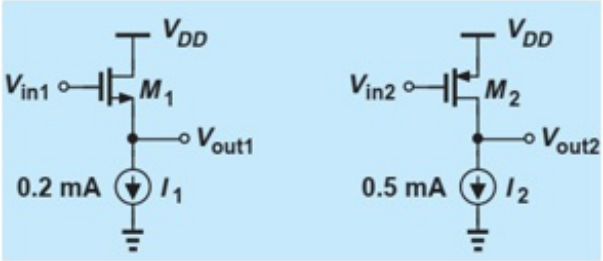

FIG.Q(1C)

2A) Design an amplifier to drive a 50Ω load with a voltage gain of 0.5 and a power budget of 10 mW. Assume $\mu_n C_{ox}$ = 100 μA/V^2, V_{TH} = 0.5 V, λ = 0 and V_{DD} = 1.8 V. (4)

2B) Assuming λ ≠ 0, compute the single-ended differential and common mode voltage gains for the circuit shown in FIG.Q(2B) using half circuit analysis. (3)

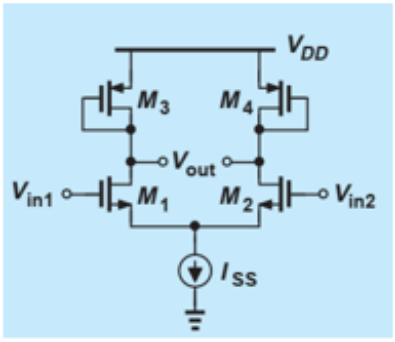

FIG.Q(2B)

2C) Design the circuit shown in FIG.Q(2C) for a voltage gain of 20 and a power budget of 1 mW with V_{DD} = 1.8 V. Assume 'M_1' operates at the edge of saturation for an input common-mode level of 1 V. Assume $\mu_n C_{ox} = 2\mu_p C_{ox}$ = 100 μA/V^2, $V_{TH,n}$ = 0.5 V, $V_{TH,p}$ = - 0.4 V, λn = 0.5 and λp = 0.1 V^{-1} (3)

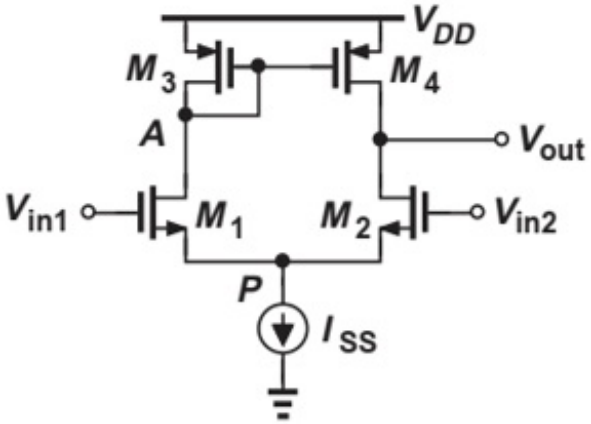

FIG.Q(2C)

3A) For the circuit shown in FIG.Q(3A), find the input and output poles at high frequencies for λ≠0. Sketch the frequency response. (4)

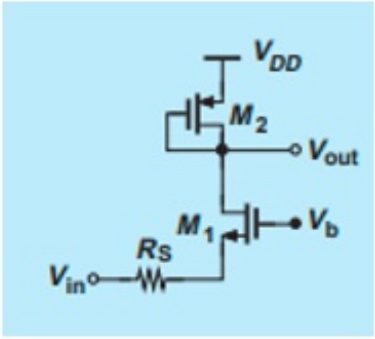

FIG.Q3(A)

3B) For the circuit shown in FIG.Q3(B), find the poles at low frequencies. Also, sketch its low frequency response. Assume λ = 0. (3)

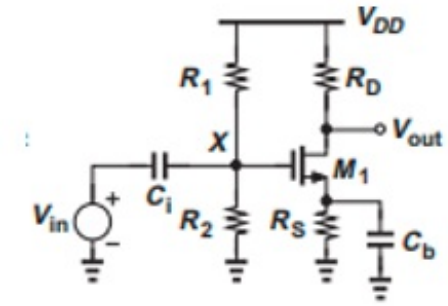

FIG.Q3(B)

3C) For the circuit shown in FIG.Q(3C), find the pole frequencies and sketch the frequency response. (3)

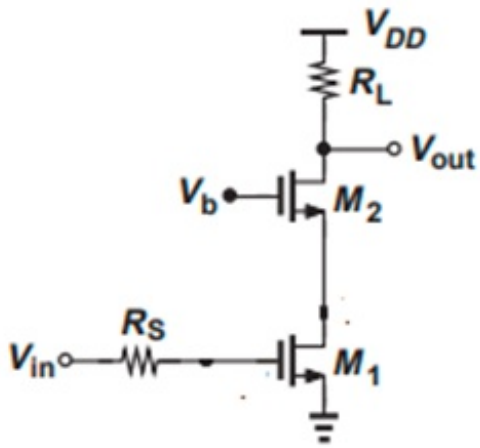

FIG.Q(3C)

4A) Determine the closed-loop gain, I/O impedance of the circuit shown in FIG. Q(4A), assuming *R1 + R2* is very large & λ=0. (4)

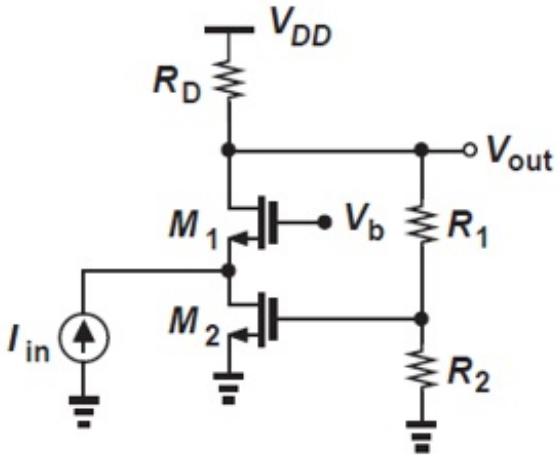

FIG. Q(4A)

4B) For the block diagram shown in FIG. Q(4B), identify the feedback topology and obtain the expressions for input and output impedance. (3)

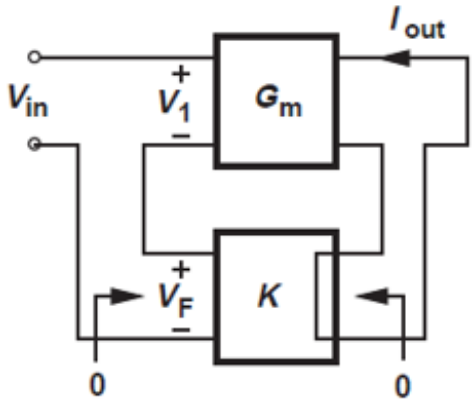

FIG. Q(4B)

4C) Determine the polarity of feedback in the circuit of FIG. Q(4C) and justify the same. (3)

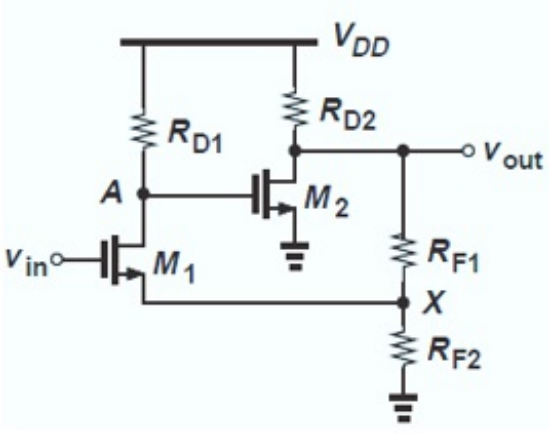

FIG. Q(4C)

5A) Explain the working principle of RC phase shift Oscillator with a neat circuit diagram. Obtain the expressions for minimum gain and frequency of oscillation. Also, find the frequency of oscillation for R=1KΩ and C=1μF. (4)

5B) Explain the working principle of ring oscillator with a neat circuit diagram. Obtain the expressions for minimum gain and frequency of oscillation. Also, find the frequency of oscillation for drain resistance and capacitance of 1KΩ and 1μF. (3)

5C) Explain the working principle of class AB amplifier with circuit diagram. (3)

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