Question Paper

Exam Date & Time: 09-Dec-2023 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

THIRD SEMESTER B.TECH. DEGREE EXAMINATIONS - NOVEMBER / DECEMBER 2023
SUBJECT: ECE 2124- DIGITAL SYSTEM DESIGN

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

Missing data may be suitably assumed.

1A) Implement f(A,B,C,D) = Σ (0,3,5,9) using optimised number 2 to 4 decoders and additional gate (4)

1B) Implement a full adder using two half-adder circuits and one OR gate (3)

1C) Implement a two input NAND gate with Transistor Transistor Logic (TTL) (3)

2A) Design a combinational circuit for conversion of code 2 4 2 1 to 8 4 2 1 code (4)

2B) Design a 3-bit asynchronous down counter using T Flip Flops. (3)

2C) Illustrate how SR flip flop can be converted to JK flip flop. Also write characteristic equations for the JK flip flop (3)

3A) Design a sequence detector to detect 1010 with overlapping using Moore model with positive edge triggered D flip flop (4)

3B) Design 4 bit universal shift register which can handle following functionalities (3)

Mode control		
S1	S0	Register operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

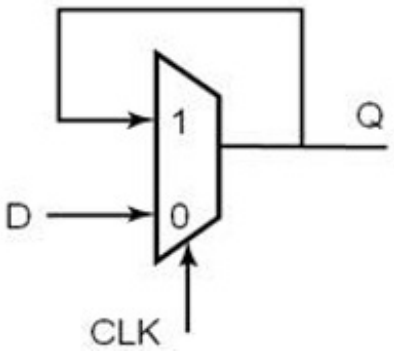
3C) Write dataflow Verilog code for the 4 to 1 Multiplexer with Delay (3)

4A) Write a structural Verilog code for 8:1 multiplexer using 2:1 multiplexer. (4)

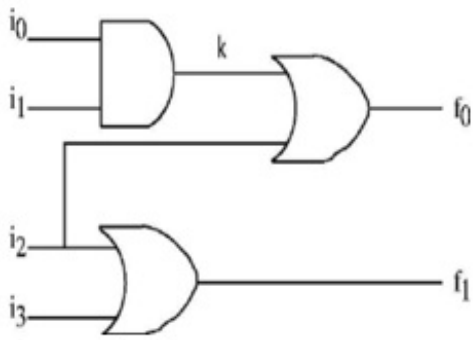
4B) Write a sequential Verilog code for 8: 3 Priority encoder using case statement (3)

4C) Write the Verilog code for a 3 input AND gate as a user defined primitive (UDP) (3)

5A) Implement the following circuit using ACT-2 Sequential module (4)



5B) Implement the following combinational circuit using Xilinx FPGA. Determine the number of CLB's and LUT's required. Show the contents in the SRAM cell. (3)



5C) Explain ASIC Design (3)

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