Question Paper

Exam Date & Time: 10-Jan-2024 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

THIRD SEMESTER B.TECH. DEGREE EXAMINATIONS - JANUARY 2024
SUBJECT: ICT 2123- DIGITAL SYSTEMS AND COMPUTER ORGANIZATION

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

1A)	If X=0, F=Y+1 otherwise F=Y-1, where X is a single bit number and Y and F are 4 bit binary numbers, design logic circuit using i) ONLY single 7483 IC ii) Minimum number of Half adders and one external gate only.	(5)
1B)	Design Full Adder using active low output 2 to 4 decoders with enable and external gates.	(3)
1C)	Construct a JK flip-flop using a D Flip-flop, a 2-to-1 line multiplexer and inverter only.	(2)
2A)	Design the circuit diagram for a sequence detector to detect a sequence 011 using Mealy model	(5)
2B)	Explain Set Associative mapping in cache memory with the help of an example.	(3)
2C)	Design a 1-bit magnitude comparator using basic gates.	(2)
3A)	Design a code converter using basic gates only to convert an 8 4 -2 -1 code to decimal digit represented in 8 4 2 1.	(5)
3B)	Devise a full adder/subtractor circuit employing a 74153 IC along with minimum XOR gates. Provide the circuit diagram and a detailed description of its operation.	(3)
3C)	Design an Asynchronous UP counter to count from 2 to 6 continuously using positive edge triggered JK - flip flops and minimum external gates.	(2)
4A)	Divide 8/3 using the restoring division approach.	(5)
4B)	Design a Synchronous counter to generate asequence: 0, 3, 5, 6, 0,.....using JK flip flops and external gates.	(3)
4C)	Draw the circuit diagram of a 2-bit Up-Down Asynchronous counter using pos-edge D flip flops and external gates.	(2)
5A)	Devise a counter circuit employing D flip-flops and minimum external gates to generate the recurrent binary sequence 0, 1, 2, 4, 6. Include the necessary connections, such as clock and clear inputs, and ensure that the counter resets to 0 after reaching 6. Illustrate your design with a state diagram, excitation table, and logic diagram. The undefined state should go to state '0'.	(5)
5B)	Design a microprogrammed control unit for 4x4 Booth's multiplier.	(3)
5C)	Explain with a neat diagram block transfer DMA technique.	(2)

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