Question Paper

Exam Date & Time: 05-Dec-2023 (09:30 AM - 12:30 PM)

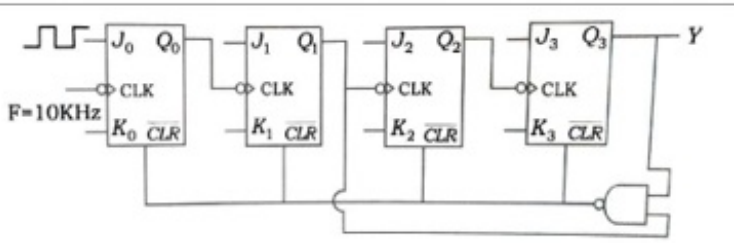
MANIPAL ACADEMY OF HIGHER EDUCATION

THIRD SEMESTER B.TECH. DEGREE EXAMINATIONS - NOVEMBER/DECEMBER 2023
SUBJECT: ICT 2123- DIGITAL SYSTEMS AND COMPUTER ORGANIZATION

Marks: 50 **Duration: 180 mins.**

Answer all the questions.

1A)	Design a 4-bit parallel adder with carry look ahead adder.	(5)
1B)	Design a full adder combinational circuit using decoder.	(3)
1C)	Convert the Jk flip flop to D Flip flop with necessary steps.	(2)
2A)	Design a sequence detector to detect three or more consecutive 1's in a sequence of bits using Mealy model	(5)
2B)	What is the role of the ALU (Arithmetic Logic Unit) in a CPU, and how does it perform arithmetic and logical operations?	(3)
2C)	Design a 4-bit by 3-bit binary multiplier and explain its operation.	(2)
3A)	Design a code converter using NAND gates only to convert a decimal digit represented in 8 4 2 1 code to a decimal digit represented in Gray code.	(5)
3B)	Design a multiplexer with a 16-to-1 configuration by using 2-to-1 multiplexers only. Illustrate the block diagram and truth table for this multiplexer design.	(3)
3C)	Design an Asynchronous DOWN counter to count from 6 to 2 continuously using negative edge triggered T-flip flops and minimum external gates.	(2)
4A)	Multiply $(-7)_{10}$ with $(3)_{10}$ by using Booth's multiplication algorithm. Give the flow chart of the multiplication.	(5)
4B)	Design a sequence generator using synchronous counter with states $0 \rightarrow 3 \rightarrow 2 \rightarrow 1 \rightarrow 0$ that generates the sequence '1100'. Use T Flip-Flop and minimum external gates.	(3)
4C)	All four flip-flops' inputs are made high in the figure below. Draw the transition diagram and find the signal's frequency at the output Y.	(2)



5A)	Design a Synchronous DOWN counter that follows a 3 - bit Gray code sequence. Illustrate the counter's operation through a state diagram, excitation table, and logic diagram. Use JK - flip flops and external gates for the design.	(5)
5B)	Explain one bus, two bus and three bus oriented RALU with neat diagrams and an example.	(3)
5C)	With neat diagrams, explain daisy chain technique for servicing multiple interrupts.	(2)

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