Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

DEPARTMENT OF MECHATRONICS ENGINEERING

III SEMESTER B.TECH. (MECHATRONICS)

END SEMESTER EXAMINATIONS, November 2023

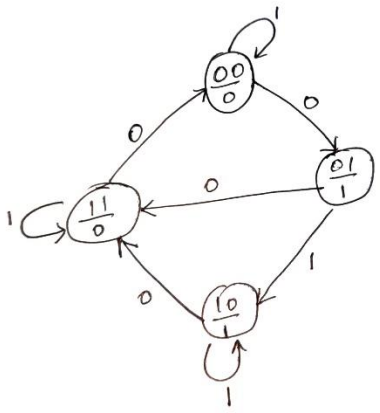
SUBJECT: DIGITAL DESIGN AND VERILOG PROGRAMMING [MTE 2122]

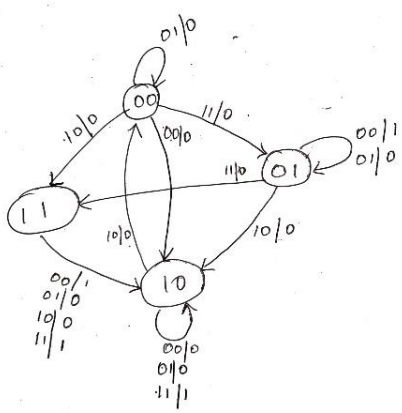
30/11/2023

Time: 3 Hours **MAX. MARKS: 50**

Instructions to Candidates:

- Answer **ALL** the questions.

Q. No		M	CO	PO	LO	BL
1A.	For the given function $f(A,B,C,D)=\overline{A}\,\overline{D}+\overline{C}\,\overline{D}+A\overline{C}D+AC\overline{D}$. i) Obtain the simplest Sum-of-Products expression ii) Implement the function using minimum number of NOR gates.	**4**	**1**	**1**	**1**	**3**
1B.	Design a synchronous counter for the sequence 0,2,3,5,7,0..using D flipflop.	**3**	**2**	**1**	**1**	**3**
1C.	Design a 4-bit BCD to excess-3 code convertor using 8:1 multiplexer. Choose any variable as MEV.	**3**	**1**	**1**	**1**	**3**
2A.	Design a sequence generator using 74LS194 IC (Universal Shift Register) to generate the following sequence 1110- 0111-1011-1101----. Repeats.	**5**	**2**	**1**	**1**	**3**
2B.	Design a mod-9 counter using IC7490	**3**	**2**	**1**	**1**	**3**
2C.	Implement a full adder using a PLA	**2**	**4**	**2**	**2**	**3**
3A.	For the state diagram of FSM shown below, design a sequential circuit using SR flipflop.  	**5**	**2**	**1**	**1**	**3**

<table>
<tr><td>3B.</td><td>Design an asynchronous mod-16 up/down counter using positive edge triggered T Flip-flop. Also draw the timing waveform.</td><td>3</td><td>2</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>3C.</td><td>A X-Y flipflop whose truth table is given below, is to be implemented using a SR flipflop. Design a suitable circuit for the same.
<table>
<tr><th>X</th><th>Y</th><th>Qn+1</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table></td><td>2</td><td>1</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>4A.</td><td>Develop a Verilog code for the state diagram shown below.

</td><td>5</td><td>3</td><td>1</td><td>1</td><td>6</td></tr>
<tr><td>4B.</td><td>Develop a Verilog code to implement a 4-bit asynchronous counter using T flipflop. The T flipflop has to be implemented using D flipflop.</td><td>3</td><td>3</td><td>1</td><td>1</td><td>6</td></tr>
<tr><td>4C.</td><td>Develop a Verilog code to implement 4:1 multiplexer using 2:1 multiplexer only. Use conditional operator for the 2:1 MUX.</td><td>2</td><td>3</td><td>1</td><td>1</td><td>6</td></tr>
<tr><td>5A.</td><td>How FPGA’s are better compared to semicustom ICs</td><td>5</td><td>4</td><td>1</td><td>2</td><td>5</td></tr>
<tr><td>5B.</td><td>Develop a Verilog code to implement a 4-bit full adder circuit</td><td>3</td><td>3</td><td>1</td><td>1</td><td>6</td></tr>
<tr><td>5C.</td><td>Develop a Verilog code to implement a 3 bit gray code converter circuit</td><td>2</td><td>3</td><td>1</td><td>1</td><td>6</td></tr>
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