Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

DEPARTMENT OF MECHATRONICS ENGINEERING

III SEMESTER B.TECH. (MECHATRONICS)

END SEMESTER EXAMINATIONS, November 2023

SUBJECT: DIGITAL DESIGN AND VERILOG PROGRAMMING [MTE 2122]

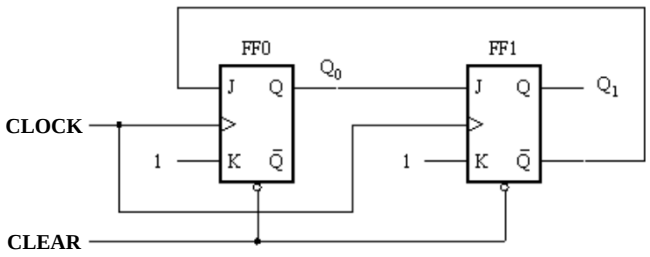
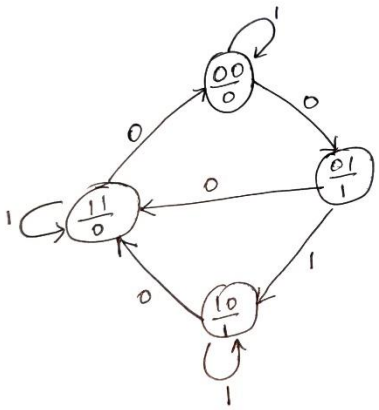
30/11/2023

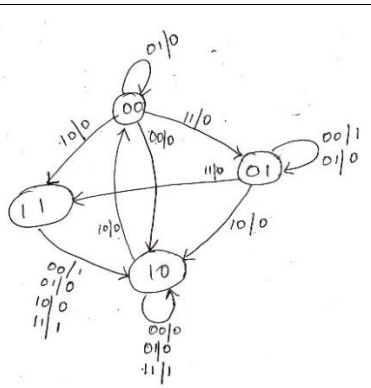
Time: 3 Hours **MAX. MARKS: 50**

Instructions to Candidates:

- Answer **ALL** the questions.

Q. No		M	CLO	PO	LO	BL
1A.	Two motors M1 and M2 are controlled by three sensors, S3, S2 and S1. One motor M2 is to run any time when all three sensors are ON (true) as well as when any two sensors are ON. M2 is also ON when only S3 is ON. The other motor M1 is to run whenever sensors S2 or S1, but not both, are ON. When all three sensors are OFF, then both motors must remain OFF. Construct a truth table and write the Boolean output equation. Implement using AND-OR circuit and NAND-NAND Circuit.	**4**	**1**	**1**	**1**	**3**
1B.	Design a synchronous counter for the sequence 0,2,5,7,3,4,0..using T flipflop. Assume that, when the supply is switched on, if the state 1 and 6 occurs, the next state would be 5.	**3**	**2**	**1**	**1**	**3**
1C.	Design a 3-bit binary to gray code converter using 4:1 multiplexer. Choose any variable as MEV.	**3**	**1**	**1**	**1**	**3**
2A.	A shift register needs to be designed to perform the following operations as shown in Table 2A. Design a suitable circuit. **Table 2A** **S1** | **S0** | **Operation** 0 | 0 | Synchronous Clear 0 | 1 | Hold 1 | 0 | Shift right 1 | 1 | Shift left	**5**	**2**	**3**	**5**	**6**
2B.	Design a two-digit counter that counts from 00 to 88 using IC 7493.	**3**	**2**	**3**	**5**	**6**

2C.	Determine the functional behavior of the circuit shown in Fig. 2C. Assume that the clock is driven by a square wave signal. Clearly mention each state with detailed analysis  **Fig. 2C**	**2**	**2**	**2**	**2**	**4**
3A.	For the state diagram of FSM shown in Fig. 3A, design a sequential circuit using JK flipflop.  **Fig. 3A**	**5**	**2**	**1**	**1**	**3**
3B.	Design an asynchronous mod-8 up/down counter using positive edge triggered T Flip-flop. Also draw the timing waveform.	**3**	**2**	**1**	**1**	**3**
3C.	A X-Y flipflop whose truth table is given in Table 3C, is to be implemented using a JK flipflop. Design a suitable circuit for the same. **Table 3C** **X** | **Y** | **Qn+1** 0 | 0 | 0 0 | 1 | Qn 1 | 0 | 1 1 | 1 | 0	**2**	**1**	**1**	**1**	**3**
4A.	Develop a Verilog code for the state diagram shown in Fig. 4A.	**5**	**3**	**3**	**5**	**6**

	 **Fig. 4A**					
4B.	Develop a Verilog code to implement a 4-bit counter based on a select line. If select=1, the counter should count up else the counter should count down. Implement using T flipflop. Draw the timing diagram	**3**	**3**	**3**	**5**	**6**
4C.	Develop a Verilog code to implement 8:1 multiplexer using 2:1 multiplexer only. Use conditional operator for the 2:1 MUX.	**2**	**3**	**3**	**5**	**6**
5A.	Compare the programming Technologies namely SRAM, Poly diffusion antifuse, EPROM, EEPROM.	**5**	**4**	**2**	**2**	**5**
5B.	Develop a Verilog code to implement a 4-bit adder/subtractor. Draw the timing diagram	**3**	**3**	**3**	**5**	**6**
5C.	Develop a Verilog code to implement a 2-bit comparator circuit. Draw the timing diagram	**2**	**3**	**3**	**5**	**6**