MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

DEPARTMENT OF MECHATRONICS

IV SEMESTER B.TECH. (MECHATRONICS)
END SEMESTER EXAMINATION

SUBJECT: Digital and Analog CMOS Design Subject Code: MTE 2123

Date: 02-12-2023

Time: 3 Hrs **Exam Time 9:30 PM – 12:30 PM** **MAX. MARKS: 50**

Name:……, Registration No:……..

- Answer **ALL** the questions.

Q. No.	Questions	M	CO	PO	LO	BL
1A	Design the following Boolean expressions with the help of two input NAND using N-MOS technology. Also, draw the NAND gate implementation of the expression. 1. $AB + \bar{B}C$ 2. $ABC + A\bar{B}C$	**4**	**1**	**2**	**2**	**6**
1B	Develop a Complementary Metal-Oxide-Semiconductor (C-MOS) circuit for a half adder. Clearly outline the organization of C-MOS components, specifying the transistor arrangement and interconnections. Also, draw its stick diagram. The color coding for the stick diagram is as follows: Polysilicon- Red, P diffusion- yellow, N diffusion- green, Metal- blue, Demarcation line- brown, Contact- black.	**4**	**1**	**2**	**2**	**3**
1C	In the context of operational amplifiers, analyze the characteristics that define a voltage feedback amplifier.	**2**	**3**	**1**	**1**	**4**
2A	Examine the procedural steps involved in the N-well process design, supported by relevant diagrams.	**4**	**2**	**1**	**1**	**4**
2B	Derive the current equation for an N-MOS transistor in the saturation region by incorporating relevant parameters and the cross-sectional view of the MOS.	**3**	**1**	**2**	**2**	**3**
2C	Construct a 2:1 multiplexer utilizing the fewest possible pass gate transistors in its configuration.	**3**	**1**	**2**	**2**	**3**
3A	Analyze the following terms in the context of CMOS fabrication technology. 1. Diffusion 2. Ion-Implantation	**4**	**2**	**1**	**1**	**4**
3B	Estimate the current 'I' flowing through the 1 kΩ resistor for the circuit shown in Figure 3B.	**3**	**4**	**2**	**2**	**5**

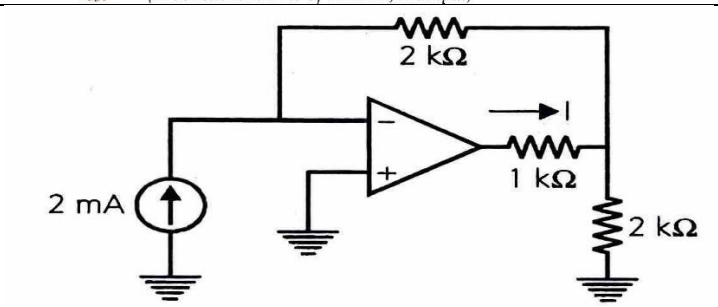
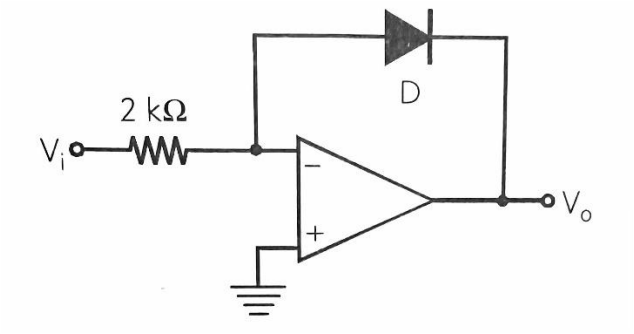
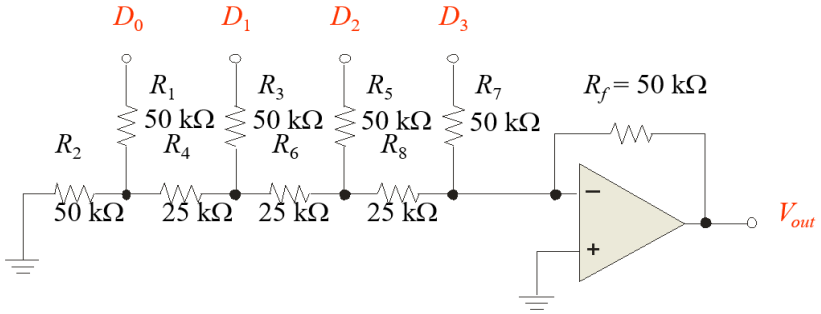
	 Figure 3B					
3C	In the op-amp circuit shown in Figure 3C, assume that the diode (D) current follows the equation $I = I_s * \exp(V/V_T)$. For $V_i = 2V$, $V_o = V_{o1}$ and $V_i = 4V$, $V_o = V_{o2}$. Determine the relationship between V_{o1} and V_{o2} .  Figure 3C	**3**	**4**	**2**	**2**	**5**
4A	Create a circuit employing a single operational amplifier to produce the specified output voltage i.e. $V_o = 3.5V_A - 7.5V_B + 5.6V_c$	**4**	**4**	**2**	**2**	**6**
4B	Analyze the operational amplifier-based sample and hold circuit with the help of supporting mathematics, suitable circuit diagram, and waveforms.	**3**	**4**	**2**	**2**	**4**
4C	Design an operational amplifier-based low pass filter at a cutoff frequency of 1 kHz, with a pass band gain of 2. Also, plot the frequency response of the filter.	**3**	**4**	**2**	**2**	**6**
5A	The R-2R ladder network is shown in Figure 5A. Determine the output voltage V_{out} if the digital input applied is 1011, the voltage corresponding to the high level is +5 V and the low level is 0 V. 	**4**	**5**	**2**	**2**	**5**

	Figure 5A					
5B	Examine the integrator circuit based on operational amplifiers, utilizing pertinent mathematical expressions and appropriate diagrams, in the given input situations. a. Unit Impulse b. Square wave	**4**	**4**	**2**	**2**	**4**
5C	Explain how the virtual ground in an op-amp different from electrical ground?	**2**	**4**	**1**	**1**	**2**