MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

V SEMESTER B.TECH. AIML

End semester Exam

SUBJECT: PARALLEL COMPUTER ARCHITECTURE AND PROGRAMMING
(CSE 3174)

Time: Date: MAX.MARKS:

Note:

1. Missing data may be assumed suitably.

Q.No	Questions	Marks	CO /CLO	AHEP LO	Blooms Taxonomy level
1A	Classify and briefly explain with diagrams how the parallel computers are categorized according to Flynn's classification.	5	1	1,3	2
1B	Solve the given scenario considering temporal parallelism. Let 2000 candidates appear for an examination. There are 5 questions in each answer script and one teacher will evaluate every question in 10 minutes. What is the time taken to correct 2000 papers in pipeline processing? Also calculate the speedup achieved.	3	1	1,3	4
1C	Illustrate any 2-deadlock scenario in point to point communication with the help of MPI code snippet.	2	2	3	3
2A	Compare the two main trajectories for designing microprocessors with diagrams by writing about the design principles.	5	3	1,5	4
2B	Design the OpenCL kernel to perform addition of 2 vectors of size N. What is the global work size if all the additions are performed in parallel? Also write only the host OpenCL API which calls the above kernel. Assume all the required objects are already created.	3	3	1,5	6
2C	Discuss the concept of platform and devices in OpenCL with the help of abstract architecture for devices.	2	3	1,5	2
3A	Design an OpenCL kernel that takes a string ***S*** and an integer variable ***Count***. Each thread should take a character of ***S*** in parallel and produce the resultant string ***RS*** by repeating that character of ***S, Count*** times as shown below. Eg : Input String ***S***: PcAp ***Count*** : 3 Output String ***RS*** : PPPcccAAAppp	5	3	1,5	6

	Write all the statements in the host that are associated with buffer for the above kernel. What is the global work size for the above kernel? Assume the *context, command_queue* objects are already created.				
3B	Illustrate the compilation process of a CUDA C program with the help of a neat diagram.	3	4	2,3	3
3C	Compare data parallelism with task parallelism.	2	4	2,3	4
4A	Design a CUDA kernel that implements sorting by counting in parallel. The basic idea behind Sorting by Counting is to count the frequency of each distinct element in the input array and use that information to place the elements in their correct sorted positions.	5	4	2,3	6
4B	Design a CUDA kernel that implements matrix multiplication using element number of threads of the resultant matrix.	3	5	2,3,5	6
4C	Compute the number of multiplication operations in a 1D convolution operation if array size is 7 and convolution mask size is 5. How many additions will be performed?	2	5	2,3,5	4
5A	Design a CUDA host and kernel code for parallel merge sort. Assume that the co-rank and sequential merge device functions are available to you.	5	5	2,3,5	6
5B	Illustrate sparse matrix vector multiplication with the help of suitable example	3	5	2,3,5	3
5C	Explore the possibility of parallelism in a convolution layer	2	5	2,3,5	6

Abbreviations:

M – Marks

CO/CLO– Course Outcome (NBA)/Course Learning Outcome (IET).

CLO – Course Learning Outcome as per AHEP 4

BT - Blooms Taxonomy Level