# End Exam Question Paper

# Semester - VII

**Department:** Electronics and Communication Engineering

**Course/Module Code:** ECE 4087

**Course Title:** System on Chip Design

**Session: July – December 2023** **Date: 10-11-2023**

**Table 1: Distribution of Marks against Course Learning Outcomes**

| CLO Statements | Course Learning Outcome | AHEP 4 | Marks |
|---|---|---|---|
| To understand the need, benefits and features of System-on-Chip against the existing technologies. | **CO1** | | 8 |
| To understand and evaluate the different features, types and choices for designing a SoC processor. | **CO2** | | 14 |
| To study in detail about the SoC implementation, Intellectual property (IP) and interconnects. | **CO3** | | 14 |
| To understand the various layers, techniques involved in SoC verification, testing and packaging. | **CO4** | | 10 |
| To extend the concept of SoC to the state of art - NoC and its various topologies and features. | **CO5** | | 4 |

**SEVENTH SEMESTER BTECH. (E & C) DEGREE END SEMESTER EXAMINATION**
**JULY-DECEMBER 2023**
**SUBJECT: System on Chip Design (ECE 4087) (PE-VI), SET-1**

**TIME: 3 HOURS** **MAX. MARKS: 50**

**Instructions to candidates**
- Answer **ALL** questions.
- Missing data may be suitably assumed.

| Q. No. | Questions | M* | C* | A* | B* |
|---|---|---|---|---|---|
| 1A | Given a set of 8 fixed (which has been placed already) Intellectual Property (IP) modules and the distances between each module, your goal is to find the shortest power signal routing possible that connects each module. Illustrate how Genetic algorithm is able to deliver effective solutions without going for an exhaustive search of Solution space when applied in this problem? Show at least two iterations. Distance between each IP module is given in the symmetrical distance matrix shown below. | 5M | **3** | | **4** |
| 1B | Evaluate an FSM implementation of a Line following robot with 2 sensor inputs and 2 outputs. Which FSM architecture do you prefer for this- a Moore or a Mealy machine. Why, explain with suitable diagrams? | 3M | **2** | | **6** |
| 1C | Illustrate with a case study the Cache Coherence Problem? How to solve the Cache Coherence problem? Give an example to achieve cache coherence through hardware? | 2M | **2** | | **2** |
| | | | | | |

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 12 | 3 | 23 | 1 | 5 | 32 | 56 |
| 2 | 12 | 0 | 9 | 18 | 3 | 41 | 45 | 5 |
| 3 | 3 | 9 | 0 | 89 | 56 | 21 | 12 | 49 |
| 4 | 23 | 18 | 89 | 0 | 87 | 46 | 75 | 17 |
| 5 | 1 | 3 | 56 | 87 | 0 | 55 | 22 | 86 |
| 6 | 5 | 41 | 21 | 46 | 55 | 0 | 21 | 76 |
| 7 | 32 | 45 | 12 | 75 | 22 | 21 | 0 | 11 |
| 8 | 56 | 5 | 49 | 17 | 86 | 76 | 11 | 0 |

<table>
<tr><td>2A</td><td>As a SoC designer of a VLSI company, you are entrusted with the task of designing and implementation of a digital security (lock) module. The machine has input button B that when pressed (B = 0 for button "0", B = 1 for button "1") causes the FSM controlling the lock to advance to a new state or in the same state. The machine can capture the 0110-overlapping sequence for allowing access to any other peripheral trying to communicate with it. Design the state diagram/FSM for the given module.</td><td>5M</td><td>2</td><td></td><td>4</td></tr>
<tr><td>2B</td><td>Explain difference between Amdahl's law and Gustafson Law?</td><td>3M</td><td>5</td><td></td><td>2</td></tr>
<tr><td>2C</td><td>Given a (scaled) speed up of 15 on 25 processors, what is the serial fraction from Amdahl’s law? A program attains 80% efficiency with a serial fraction of 4%. Approximately how many processors are being used according to Amdahl’s law?</td><td>2M</td><td>5</td><td></td><td>2</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>3A</td><td>As a System on Chip Physical designer, you are assigned to do the driver placement, to minimise the wirelength of the clock network by reducing the distance between flip-flops and their drivers- the clock buffers. The idea is to form flip-flops into groups, such that clock buffers can be placed judiciously, reducing the overall clock-network wirelength and achieving significant power saving. There are two clock buffers and 10 Flipflops. Select any algorithm and optimize the locations of the two clock drivers. The fixed coordinates of the flip-flops are given in the Table below. Show at least two iterations.
<table>
<tr><th>X position</th><th>Y Position</th></tr>
<tr><td>0</td><td>5</td></tr>
<tr><td>2</td><td>5</td></tr>
<tr><td>1</td><td>3</td></tr>
<tr><td>4</td><td>0</td></tr>
<tr><td>1</td><td>2</td></tr>
<tr><td>2</td><td>4</td></tr>
<tr><td>2</td><td>2</td></tr>
<tr><td>3</td><td>2</td></tr>
<tr><td>3</td><td>1</td></tr>
<tr><td>4</td><td>5</td></tr>
</table></td><td>5M</td><td>4</td><td></td><td>4</td></tr>
<tr><td>3B</td><td>Find the minimum number of Test vectors to detect faults at following input points (i) P (ii) Q (iii) R and (iv) S as shown in the Fig below.</td><td>3M</td><td>4</td><td></td><td>3</td></tr>
</table>

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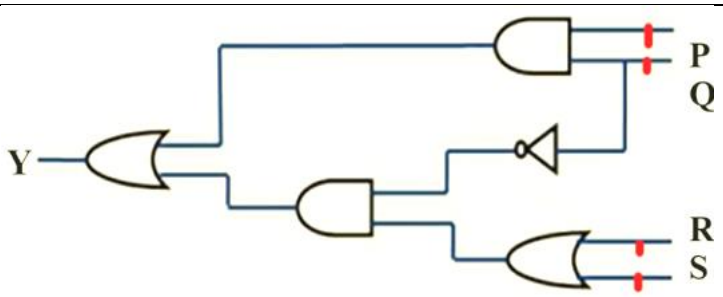
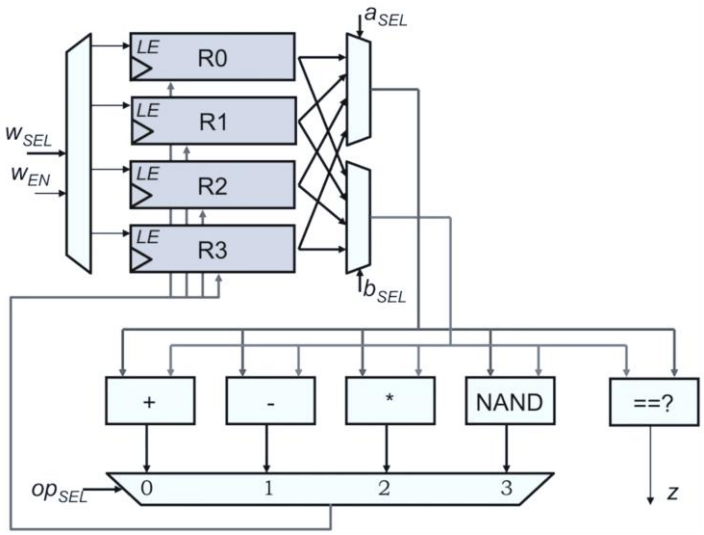
|---|---|---|---|---|---|
| |  | | | | |
| 3C | What are the different components of a Semiconductor Intellectual Property (IP)? Explain IPs at different levels-Device, Cell and System level? | 2M | **3** | | **1** |
| | | | | | |
| 4A | Design the control flow and control signals required to configure this programmable Datapath given in the Figure to perform factorial operation. You may add more hardware modules. Assume missing data if necessary.<br>  | 5M | **2** | | **5** |
| 4B | Explain the process of Floor planning in a System on a chip design flow? What are the objectives of a Floorplan process?<br><br>A chip with a poor Floorplan is shown below. Redo the Floor Plan and calculate the improvement and utilization after that. Assume no constraints in the blocks and pin connections. | 3M | **4** | | **3** |

| | | | | | |
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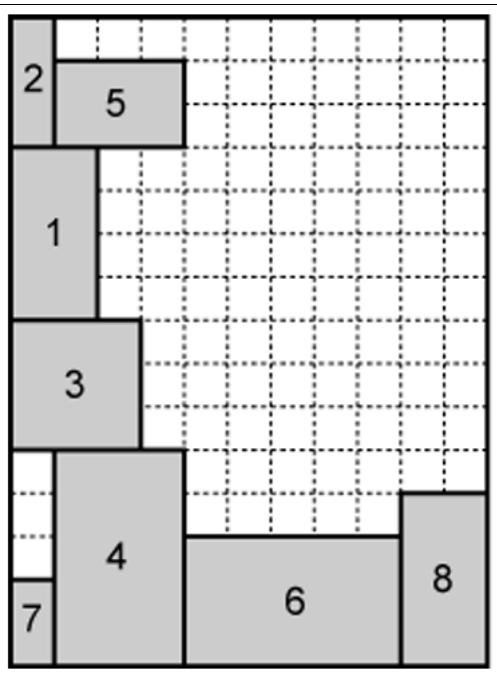
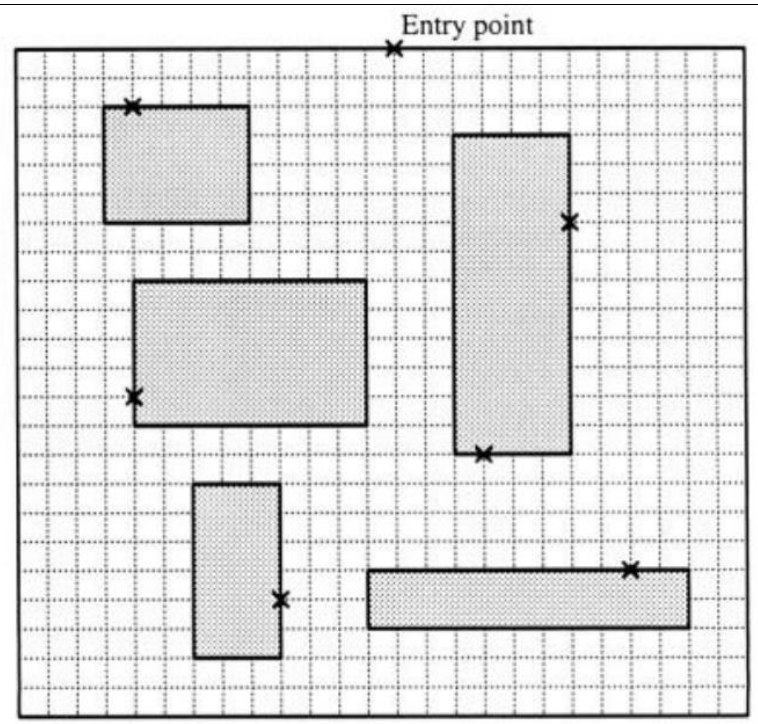
| |  | | | | |
| 4C | While designing a SoC, a module needs to perform multiply, divide, add operations with a stream of numbers given by the function O=(a*b*c+d*e)/f+g*h.<br>Compute the maximum clock frequency of the system with pipelining, given below the delay of each unit? What is the Speed up? Suggest some ways to improve the present operating frequency.<br>The Delays for the Adder, Multiplier, Divider are 10ns, 25ns and 40ns respectively. | 2M | **2** | | **2** |
| | | | | | |
| 5A | As a System-on-Chip architect you are assigned to design an Exponentiation module to find the product of two numbers input by the user, use registers, adder/subtraction, multipliers, comparator and other common digital blocks only. Design an optimized Datapath for this module. | 5M | **4** | | **5** |
| 5B | Model a state diagram for the machine representing the controller of the Exponentiation module. Show the different states and control outputs issued in each state of the FSM designed for the Exponentiation module. | 3M | **2** | | **4** |
| 5C | What do you mean by Clock skew? What are the challenges of having high skew? Figure shows a partial layout of a chip. Complete the layout of chip by clock routing- connecting the clock signal source from the entry point to all the terminals of IP modules (marked as ‘x’) as shown in the Figure below, so that clock skew is minimized. | 2M | **4** | | **2** |

| | | | | | |
|---|---|---|---|---|---|
| |  | | | | |

**M*--Marks, C*--CLO, A*--AHEP LO, B* Blooms Taxonomy Level**