



DEPARTMENT OF SCIENCES
I SEMESTER M.Sc. (PHYSICS)

END SEMESTER REGULAR EXAMINATIONS, NOVEMBER & DECEMBER 2023
FUNDAMENTALS OF ELECTRONICS [PHY 5154]
(CHOICE BASED CREDIT SYSTEM - 2020)

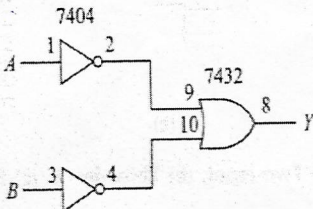
Time: 3 Hours

Date: 06-12-2023

MAX. MARKS: 50

Note (i) Answer ALL questions

(ii) Draw diagrams, and write equations wherever necessary

		Marks	CO	BL																								
1A	(a) For a given CE base configuration of transistor sketch the ac equivalent using r_e model by replacing transistor. (b) Explain different methods by which SCR can be turned on.	2 3	1	1																								
1B	(a) Draw the basic construction of a n -channel JFET. (b) Apply the proper biasing between drain and source and sketch the depletion region for $V_{GS} = 0$ V.	1.5 1.5	1	3																								
1C	Given $I_D = 14$ mA and $V_{GS} = 1$ V, determine V_P if $I_{DSS} = 9.5$ mA for a depletion-type MOSFET.	2	1	3																								
2A	Explain the working of inverting amplifier using opamp with proper circuit diagram and arrive to the expressions of closed loop gain, bandwidth with feedback and output resistance with feedback	5	1	1																								
2B	Obtain frequency response data as shown below: for the first order low pass filter with a cutoff frequency 2kHz and pass band gain 1. Construct the frequency response plot from the following data. <table><tr><th>Frequency</th><th>Gain Magnitude</th><th>Magnitude (dB)</th></tr><tr><td>10</td><td></td><td></td></tr><tr><td>100</td><td></td><td></td></tr><tr><td>500</td><td></td><td></td></tr><tr><td>1000</td><td></td><td></td></tr><tr><td>2000</td><td></td><td></td></tr><tr><td>5000</td><td></td><td></td></tr><tr><td>10000</td><td></td><td></td></tr></table>	Frequency	Gain Magnitude	Magnitude (dB)	10			100			500			1000			2000			5000			10000			3	1	3
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10																												
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2C	What are the two basic modes in which the 555 Times operates.	2	1	2																								
3A	(a) What is the NAND-NAND circuit for $Y = AB + AC + AD + BCD$. (b) Write down truth table and timing diagram for the following gate circuit. <div></div>	2 2 2	2	3																								

3B	<p>(a) Draw Karnaugh map for $F(A, B, C, D) = 1$ (1,3,8,9, 10, 14,15) and write the simplified Boolean equation for the same.</p> <p>(b) Convert decimal 108.364 to a binary number. - Convert the following hexadecimal numbers to binary numbers: i. E5 ii. B4D</p>	2	2	3
3C	Mention different types of instructions used in 8085 microprocessor	2	2	2
4A	<p>Using the following negative edge triggering at RS FF, explain the changes in output Q at different instant of time.</p>	3	2	4
4B	Design 4 to 1 line multiplexer (MUX) with truth table & logical circuit diagram.	4	2	6
4C	<p>(a) Load 63H in memory location 2001H and increment the contents of memory location.</p> <p>(b) Load 48H in 2000H and increment the contents of memory location along with status of registers. Assume the contents of accumulator are 4CH and CY=1. Illustrate the accumulator contents after the execution of the instruction RAL.</p>	1	2	6
5A	Explain briefly architecture of 8085 μ p with diagram.	5	2	1
5B	A count 35H is loaded in register C & loop is executed until count reaches zero. Write flowchart and program to set up the loop. Calculate time delay in the loop with clock frequency 4MHz. (Total T-states for loop are 14)	2	2	5
5C	Load hexadecimal numbers 7CH and B2H in registers B and C. If sum is greater than FFH display 02H at output port 2 otherwise display the sum on o/p port 1 along with flowchart mention the number of memory locations occupied by this program.	3	2	6
