Question Paper

Exam Date & Time: 23-Nov-2023 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
First Semester Master of Engineering - ME (VLSI Design / Microelectronics and VLSI Technology/ Embedded Systems) Degree Examination - November / December 2023

System on Chip Design [VLS 5132]

Marks: 100 **Duration: 180 mins.**

Thursday, November 23, 2023

Answer all the questions.

1)	Explain and analyze the architectural view of simple sequential and pipelined processor models with neat diagrams CO1, PO3, BL4	(10)
2)	Classify the advantages and disadvantages of implementing an application in hardware and software? Explain codesign space with a neat diagram. CO1, PO3, BL2	(10)
3)	Describe briefly about post-partitioning analysis and debug in ESL flow CO1, PO3, BL4	(10)
4)	Demonstrate the block diagram of a Portable Multimedia System and explain the Design Principles involved in the SoC CO1, PO3, BL4	(10)
5)	Sketch the basic elements in instruction handling with neat diagrams CO2, PO4, BL3	(10)
6)	Sketch the block diagram of a superscalar processor and explain. Discuss three types of dependencies and the methods of solving them CO2, PO4, BL3	(10)
7)	Solve the following: A set associative cache has total of 64 blocks divided into sets of 4 blocks each. a) Main memory has 1024 blocks with 16 words per block. How many bits are needed in each of the tag, index and word fields of the main memory address? b) A computer system has 32K words of main memory and a set associative cache.	(10)

The block size is 16 words and the tag field of the main memory address is 5 bits wide. If the same cache is direct mapped, the main memory will have a 3-bit tag field. How many words are there in the cache? How many blocks are there in a cache set? CO2, PO4, BL3

8) Explain fully associative mapping, Direct mapping, and Set associative mapping in cache organization with the help of examples. Consider a typical segment table as shown below (all the values are in hex-decimal format) (10)

Segment No.	Segment Base Address	Segment Length
0	0D1	258
1	8FC	00E
2	05A	064
3	052F	244

The virtual address format is 3 bits for segment and 9 bits for offset
Evaluate out the physical address for the following logical address
a) 20B b) 790 c) 590 CO2, PO4, BL3

9) Describe at least 2 different static and dynamic network on chip concept. Explain base line network topology with a relevant example. CO3, PO4, BL2 (10)

10) Describe memory-mapped interface, coprocessor interface, and custom-instruction interfaces with relevant diagrams and examples. CO3, PO4, BL2 (10)

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