Question Paper

Exam Date & Time: 25-Nov-2023 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
First Semester Master of Engineering - ME (Microelectronics and VLSI Technology) Degree Examination - November / December 2023

Digital VLSI Design [MVT 5102]

Marks: 100 **Duration: 180 mins.**

Saturday, November 25, 2023

Answer all the questions.

1)	Explain the possible crystal defects and their effects after the crystal is grown.	(10)
2)	Explain the thermal oxidation mechanism.	(10)
3)	What are the important second order effects in MOSFETs? Explain them briefly.	(10)
4)	Explain the operation of a CMOS inverter, showing different regions of operation.	(10)
5)	What are the ways of constructing a large inverter? Explain with layouts.	(10)
6)	Derive a complete low frequency, small signal model for a MOSFET with bulk effect.	(10)
7)	Give the detailed design of a CMOS D flip-flop. Using multiplexers and this D flip-flop how do you design a 4-bit synchronous binary counter? Explain its working.	(10)
8)	Deduce the analytic delay models for the: (4 + 4 + 2) a) Fall Time b) Rise Time c) Delay Time	(10)
9)	Design a CMOS circuit for the Boolean expression F = ((A.B + C) D.E)' with equal rise time (t_r) and fall time (t_f).	(10)
10)	a) Explain briefly, the CMOS domino logic with an example. How can this be converted into a static one? b) What is a C^2MOS logic? Explain with a neat diagram.	(10)

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