Question Paper

Exam Date & Time: 29-Nov-2023 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
First Semester Master of Engineering - ME (VLSI Design / Microelectronics and VLSI Technology) Degree Examination - November / December 2023

Verification [VLS 5103]

Marks: 100 **Duration: 180 mins.**

Wednesday, November 29, 2023

Answer all the questions.

1) Describe verification challenges with respect to Size or number of designs, Complexity of the design, Verification Process being used. (10)

2) Describe linting and simulation in verification technology. (10)

3) Define Verification Productivity and briefly explain the different ways to improve the productivity of a verification project. (10)

4) Compare Platform-based Verification and System-Interface Driven Verification with diagrams. (10)

5) Illustrate a minimum of 5 possible test cases to be involved in verifying the following protocol. (10)

A synchronous system with active low *reset* consists of a transmitter and a receiver synchronizes with positive edge of the *clock*. The data is sent when *ready* is active low and *valid* is active high. While receiving the data, *valid* is active low and *ready* is active high. The maximum size of the data is 32 bits, the transfer can be either parallel or serial 1 bit at a time. The transmitter goes into high impedance during reset.

Arrange the answers in a tabular format as shown below

Testcase Name	Input Condition	Expected Output
1.		
2.		
3.		
4.		
5.		

6) Design an ALU module that performs Addition, Subtraction, AND, NOT, and OR operations. Provide code snippets for verification sequences and properties of any three operations and bug detection. (10)

7) (10)

	Analyze the various layers of the testbench architecture; explain the same with diagram. List out any five rules associated with a verification testbench architecture.	
8)	What are the two types of random properties supported by OOP-based randomization? Demonstrate the use with a random example code and appropriate output.	(10)
9)	Describe timing resolution issues in testbenches with appropriate examples.	(10)
10)	Define coverage driven verification. Compare directed verification and constraint-driven random verification	(10)

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