Question Paper

Exam Date & Time: 25-Nov-2023 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
First Semester Master of Engineering - ME (VLSI Design) Degree Examination - November / December 2023

Digital Systems and VLSI Design [VLS 5102]

Marks: 100 **Duration: 180 mins.**

Saturday, November 25, 2023

Answer all the questions.

1)	With the relevant figures explain the different steps in raw wafer preparation.	(10)
2)	List and explain the uses of S_iO_2 layer.	(10)
3)	Compare positive and negative photoresists.	(10)
4)	Deduce the relationship between Voltage and current in a MOSFET at different regions of operation.	(10)
5)	Explain the operation of a CMOS inverter, showing different regions of operation.	(10)
6)	Describe transistor sizing? What is its importance? Explain the T-sizing of the following Boolean expression: Z = ((A.B + C) D)'	(10)
7)	Give the detailed design of a CMOS D flip-flop. Using this, how do you design a 4-bit asynchronous binary counter? Explain.	(10)
8)	Design a fully complimentary single bit full adder using minimum number of transistors. Using this adder, explain how do you construct an adder/subtractor circuit.	(10)
9)	List the various components of CMOS power dissipation? Deduce expressions for each of these components.	(10)
10)	a) Explain briefly, the CMOS domino logic with an example. How can this be converted into a static one? b) Describe a C^2MOS logic? Explain with a neat diagram.	(10)

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