Question Paper

Exam Date & Time: 27-Nov-2023 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
First Semester Master of Engineering - ME (VLSI Design / Microelectronics and VLSI Technology) Degree Examination - November / December 2023

High Level Digital Design [VLS 5001]

Marks: 100 **Duration: 180 mins.**

Monday, November 27, 2023

Answer all the questions.

1) Solve the following by converting them to single precision floating point numbers. (10)

- 0.525 - 0.325
- 0.75 X (- 0.125). CO1, PO3, BL3

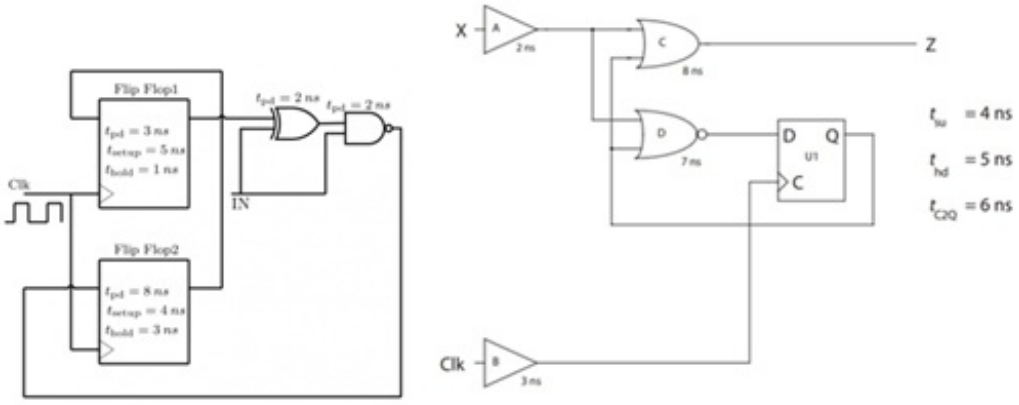
2) Apply the combinational logic design to detect a given number is between 5 to 13 when the input is 4-bit. Also draw the optimal circuit. CO1, PO3, BL3 (10)

3) Demonstrate funnel shifter design to shift 4-bits input with relevant explanation. CO2, PO3, BL3 (10)

4) Design and draw the circuit for a divided by 4 clock frequency circuit and explain its working principle. CO3, PO3, BL6 (10)

5) Design and draw a combined Moore FSM for detecting the sequences 001 and 100. Optimize the states using implication method and draw the circuit. CO3, PO3, BL6 (10)

6) Solve for total delay of the circuit (a) and hold slack for circuit (b) (10)



(a) (b)

CO3, PO3, BL3

7) Demonstrate the design of an asynchronous FIFO with a schematic diagram. (10)
CO4, PO4, BL3

8) Describe the Configurable Logic Blocks and Configurable I/O Blocks in in a CPLD. List the important pros and cons of FPGAs. CO4, PO4, BL2 (10)

9) Describe with relevant diagrams, the anti-fuse and SRAM programming technologies in FPGAs. CO4, PO4, BL2 (10)

10) Organize the AMBA APB for a write and read transfer with the help of finite state machine and relevant timing diagrams. (10)
CO5, PO4, BL4

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