Exam Date & Time: 07-May-2024 (02:30 PM - 05:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

FOURTH SEMESTER B.TECH. (ELECTRONICS AND COMMUNICATION ENGINEERING)
DEGREE EXAMINATIONS - APRIL / MAY 2024
SUBJECT: ECE 2223/ECE_2223 - ANALOG INTEGRATED CIRCUITS

ANALOG INTEGRATED CIRCUITS [ECE 2223]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

Missing data may be suitably assumed.
Assume OPAMP saturation voltage to be ±12V, if not mentioned in a particular question.

1A) Estimate V_0 expression for the circuit shown in Fig. 1(A). (4)

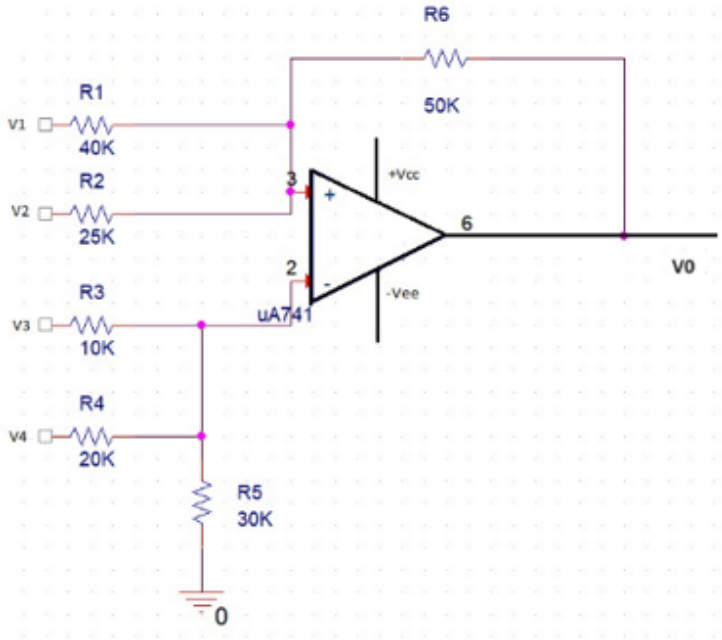


Fig. 1(A)

1B) In the circuit of Fig. 1(B) specify suitable component values to achieve a sensitivity of 0.1 V/nA. (3)

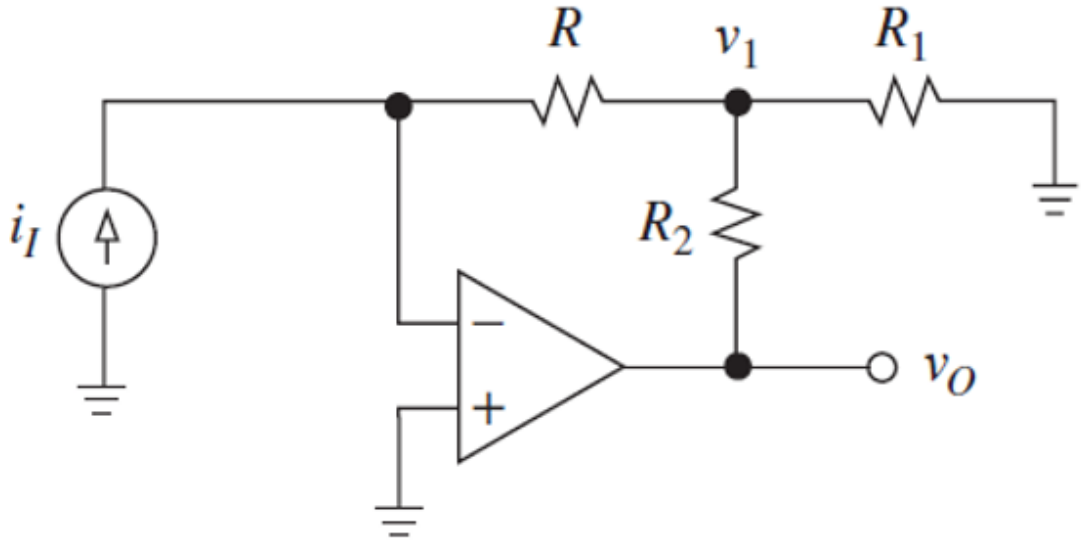
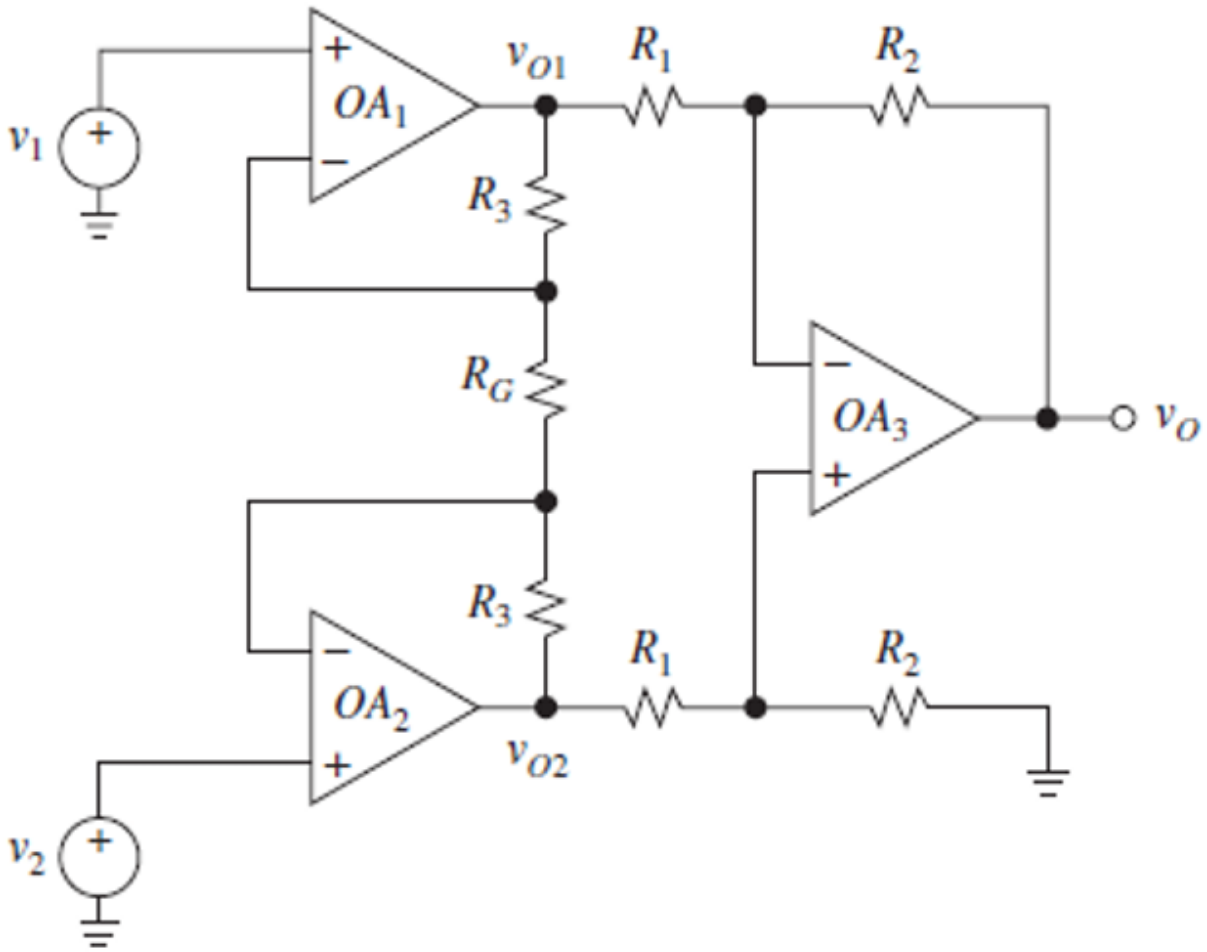


Fig. 1(B)

1C) For the instrumentation amplifier,(i) interpret the expression for the output voltage. (ii) Solve the output voltage for the circuit shown in Fig. Q1C. with R1=50KΩ, R2 = R3 = RG = 25KΩ.



(3)

Fig. 1(C)

2A) Design a 4th order Butterworth LPF with fc =1KHz and passband gain of 5. (Take C=0.1μF). (4)

2B) Explain the working of the circuit shown in Fig. Q2B. Draw the transfer characteristics and sketch the output of the circuit if a 2-volt, peak-to-peak sinusoidal input is given as input. Consider the diode as ideal and resistances $R_1 = R_2$ and $\pm V_{sat} = \pm 12$ V. (3)

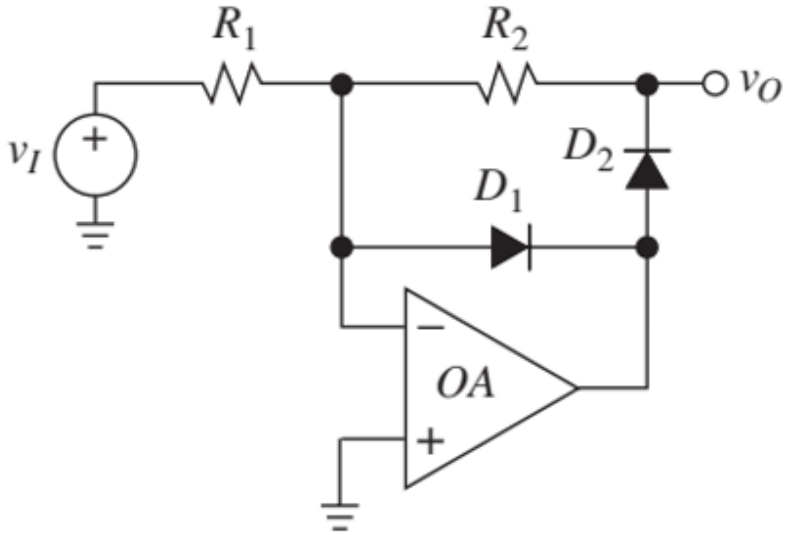


Fig. Q2B

2C) The input signal shown in Fig. Q2C is applied to the comparator. Draw the output showing its proper relationship to the input signal. Assume the maximum output levels of the comparator are ± 12 V. (3)

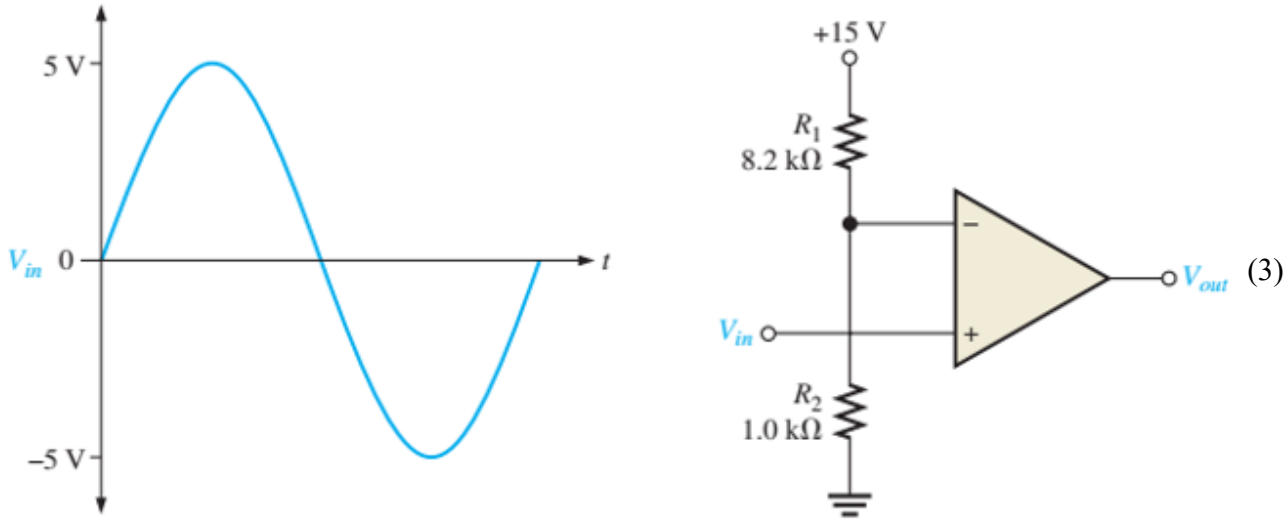


Fig. Q2C

3A) Implement a square wave generator for 1KHz frequency. (4)

3B) In the circuit of Fig. 3(B) let R = 330 kΩ, C = 1 nF, R_1 = 10 kΩ, and R_2 = 20 kΩ. Assuming ±15V supplies, find f_0 and D(%) if a third resistance R_3 = 30 kΩ is connected (3)

between the noninverting-input pin of the 301 and the −15V supply.

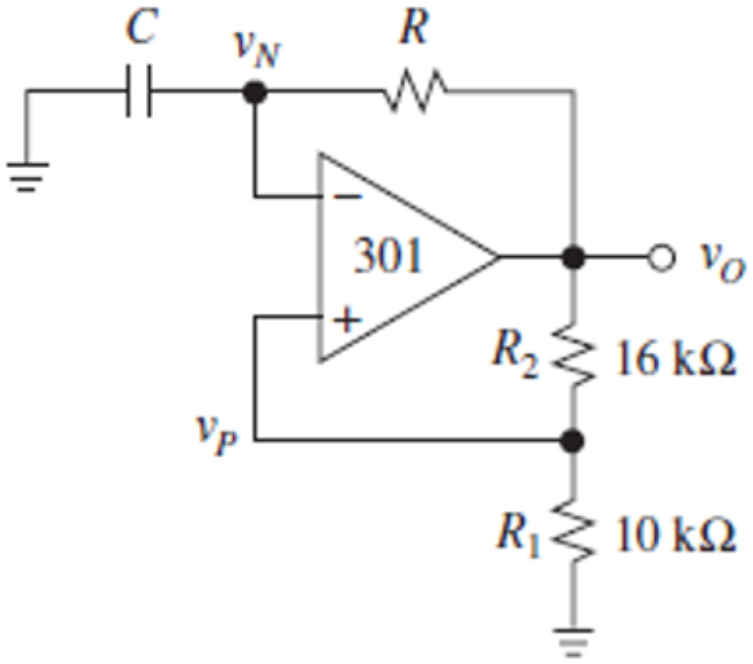


Fig. 3(B)

3C) Implement a 555-timer based circuit to give a square waveform of 1KHz frequency and adjustable duty cycle between 35% to 65%. (3)

4A) If Vcc = 6V and V_I=3+3Sinπt. Determine & sketch the output of the circuit of the circuit shown in Fig. Q4A. (4)

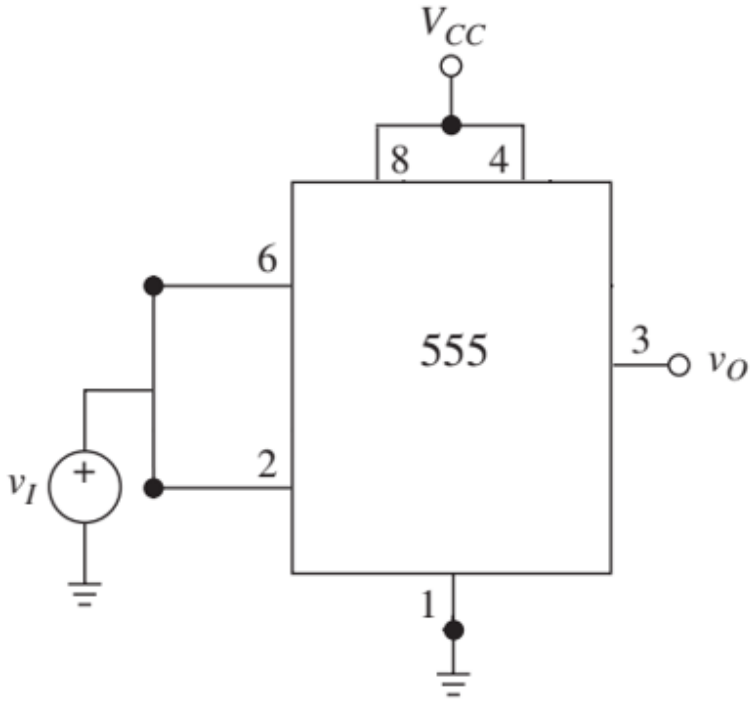


Fig. Q4A

4B) The circuit shown in Fig. Q4B has R_f=R and V_I=2V. Determine the output of the circuit, if 11000111 is digital input at D. (3)

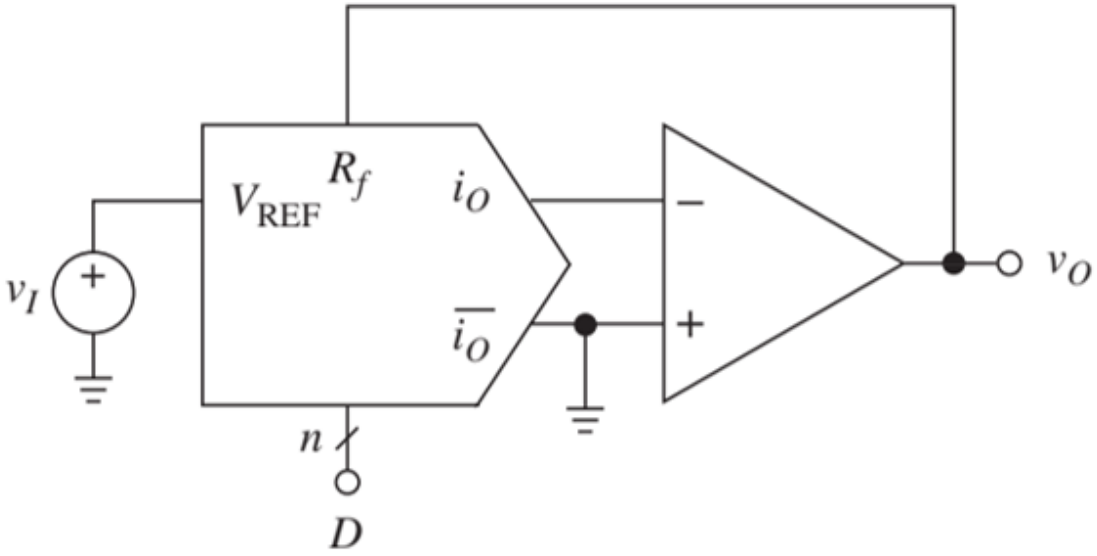


Fig. Q4B

4C) Calculate output frequency f_0, lock range Δf_L and capture range Δfc, of 565 PLL if R_T = 10 kΩ, C_T = 0.01 μF and C = 10 μF. (3)

5A) Explain the working of dual slope ADC with neat diagram. A dual slope ADC uses an 8-bit counter and 4MHz clock. The maximum input voltage is 5V and maximum output voltage should be -8V. Design a ADC circuit assuming the capacitor to be 0.01μF. (4)

5B) Draw the circuit diagram of 4-bit R-2R resistor type DAC. Determine the output when (i) b3b2b1b0 = 0100. Select R=10KΩ, Rf = 20KΩ. Logic 0=0V and logic 1=5V. (3)

5C) Draw the basic block diagram of VCO and explain. Derive the expression for free running frequency. (3)

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