Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

VI SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

MAKE-UP EXAMINATIONS, JUNE 2024

FPGA BASED SYSTEM DESIGN [ELE 4063]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: June 2024** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

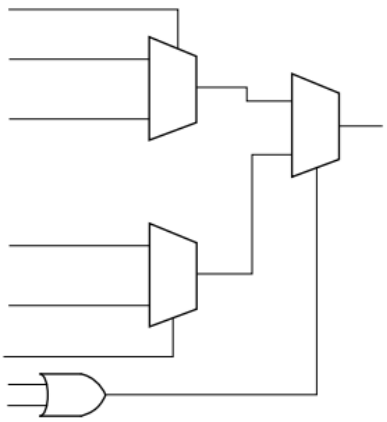
1A Explain with circuit EPROM programming technology. Mention the important features of this technology. ***03***

1B Analyze the Verilog code given below to construct the synthesized circuit. For addition and comparison operations use adder and comparator blocks.

```
module addborcb(x, a, b, c, d);
input wire [15:0] a, b, c;
input wire d;
output reg [15:0] x;
reg [15:0] t;
always @ ( a or b or c or d ) begin
if ( d ) t = b; else t = c;
if ( a < 8 ) t = t + 12;
x = a + t;
end
endmodule
```

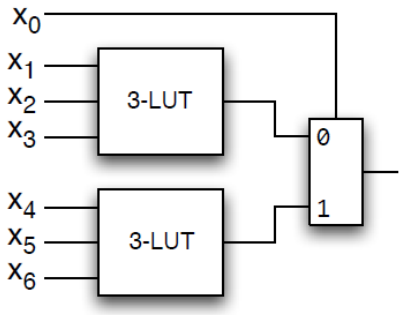
03

1C Implement the sum Boolean function of full adder using ACT-1 module. ACT-1 module is given below.



04

2A The configurable logic block (CLB) of an FPGA is shown in the Figure. Show the implementation for 8:1 multiplexer using only CLBs of this FPGA. Use minimum number of CLBs. Give the contents of all the LUTs. Mention the number of CLBs used.



04

2B Compare the techniques used for fast reconfiguration in case of partial reconfiguration. ***03***

2C Design an LFSR (pseudo-random number generator) with n=4 that generates a maximum length sequence. Add logic so that 0000 is included in the state sequence. Determine the actual state sequence. ***03***

3A Design a digital system with the RTL based approach. Digital system has the following input, output and functional descriptions.

X: 8-bit input to the system

D: single bit input to the system

R: single bit input to the system

S: 32-nit output from the system

Functional description of the system:

On every clock cycle, if D=1, the system should add X to a running sum and output that sum on S. If D=0, the system should subtract X from a running sum and updated the result on S. When R=1, the system should clear its sum back to 0. Ignore the issues of overflow and underflow.

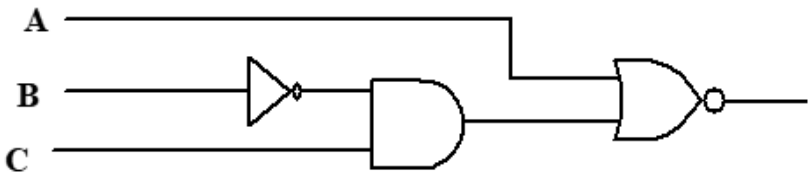
Use the RTL based approach to develop the digital system. Provide only the data path and the required finite state machine.

You are allowed to make any appropriate assumption.

04

3B Write Verilog test bench code for half adder. Display the message "error" if half adder outputs are not matching with expected functionality. Assume the Verilog code for the design under test is available with necessary input and output. ***03***

3C For the circuit given below determine the set of test vectors that detect only all stuck-at-0 faults in the circuit. Make sure to use the minimum number of vectors.



03

4A For each of the system constraints below, choose the most appropriate technology from among FPGA, standard cell, and full-custom IC technologies for implementing a given circuit. Justify your answers.

i. A system must exist as a physical prototype by next week
ii. The system should be as small and low-power as possible. Short design time and low cost are not priorities.
iii. The system should be reprogrammable even after the final product has been produced.
iv. The system should be as fast as possible and should consume as little power as possible, subject to being completely implemented in just a few months. ***04***

4B Create a FPGA based circuit to implement 16 input NOR gate. Every CLB of FPGA has the following architectures.

i. 4 numbers of 4 input LUT.
ii. Carry and control Logic

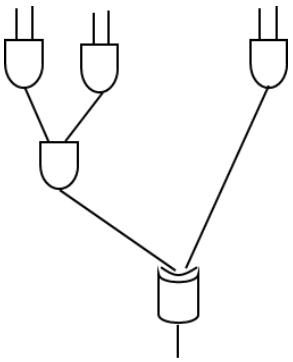
The implemented circuit should have minimum numbers of CLBs. Determine the number of CLBs used and logic levels. ***04***

4C Discuss the functionalities of Delay Locked Loop (DLL). ***02***

5A Choose the best LUT to implement the logic circuit given below. Choices available are

(i) 5 input, 1 output LUT with delay of 2 ns
(ii) 6 input, 1 output LUT with delay of 3 ns

Assume 6 transistors are used to implement SRAM cell.



02

5B Part of state transition table of FSM is given in Table. Predict the timing diagram for testing FSM using scan path test.

Present state	Next state $Q_1^+Q_2^+Q_3^+$		Output Z	
Q1 Q2 Q3	X=0	X=1	X=0	X=1
100	110	111	1	0

04

5C A FIR low pass first order digital filter is designed to process speech signal with cut-off frequency of 8.5 kHz. The designed filter has impulse response h[n] = [5, 7]. Build an appropriate structure using the resources available in FPGA for the implementation of FIR low pass filter. Determine output y[3] for the input x(n) = [7, 1, 3]. Clearly mention the partial output for each bit shift of the shift register. ***04***