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MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

VI SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)
END SEMESTER EXAMINATIONS, MAY 2024

FPGA BASED SYSTEM DESIGN [ELE 4063]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 06 May 2024** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A Explain with sketches an Antifuse programming technology. ***03***

1B Analyze the Verilog code given below to construct the synthesized circuit. For multiplication and addition operations use multiplication and adder blocks. Also, estimate the latency.

```
module example (
output reg [7:0] XPower,
input clk,
input [7:0] X
);
reg [7:0] XPower1, XPower2;
reg [7:0] X1, X2;
always @(posedge clk) begin
X1 <= X;
XPower1 <= X;
X2 <= X1;
XPower2 <= XPower1 * X1;
XPower <= XPower2 * X2;
end
endmodule
```

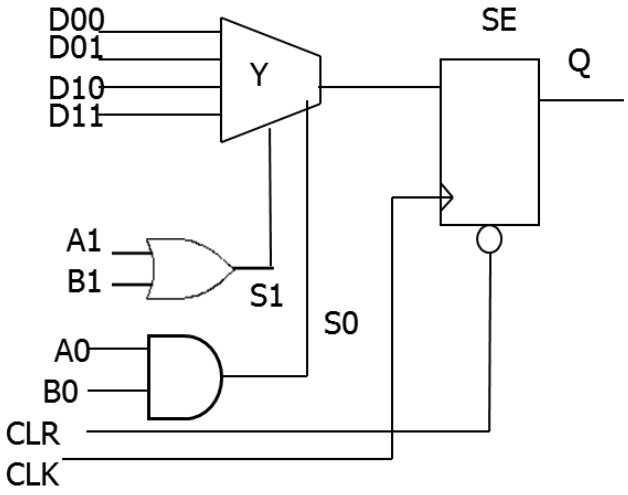
03

1C Develop a universal 4-bit shift register using minimum numbers of ACT-3 S Module. The shift register function table and ACT-3 S module are given below.

Selection input	Operation
00	Clear
01	Load data
10	Left shift
11	Right shift

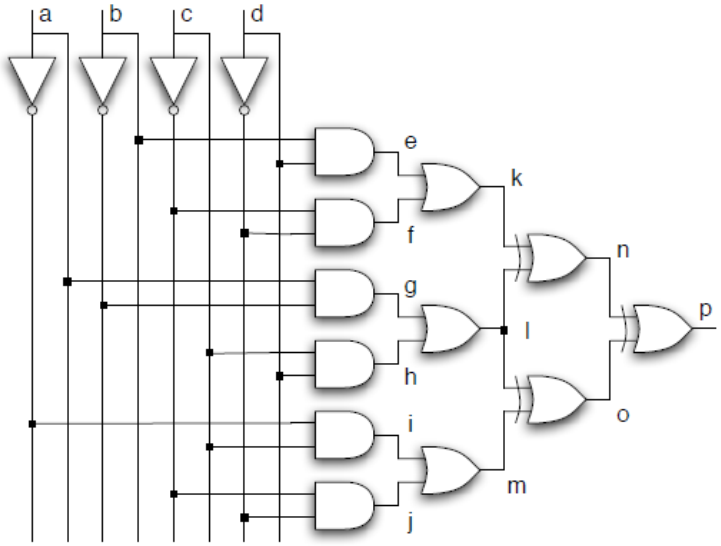
04

S-Module (ACT 3)



2A Using only 4-input lookup tables (LUTs), partition the circuit shown below into as few LUTs as possible. Do not attempt to simplify the gate-level circuit before mapping it to LUTs. Indicate

your answer by filling in the table. Fill in one row for each LUT, assigning node names from the circuit to LUT inputs and outputs. Mark unused LUT inputs with "X" (for unused). Estimate the content (bits) of LUT with output P.



LUT #	input 1	input 2	input 3	input 4	output
1					
2					
3					
4					
5					
6					
7					
8					

04

2B Explain partial reconfiguration design flow with flow chart. ***03***

2C Design a hardware-based input stimulus generation circuit (random number generation circuit) to test a collision detection circuit with the following function. A network router connects 3 computers together and allows them to send messages to each other. If two or more computers send messages simultaneously, they collide and messages must be resent. Collision detection circuit generates high output if two or more computers send messages simultaneously. Determine all the random numbers generated by the designed circuit. ***03***

3A Construct data-path and control unit for a processor with the following three instructions.

i. Load instruction: Load the data from data memory to one of the registers in register file

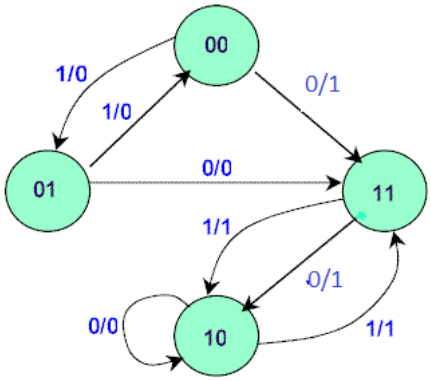
ii. Store instruction: Store the data from any register in the register file to any data memory location

iii. Multiply instruction: Multiply the data present in two registers and write result back to one of the registers

Mention the assumptions made. ***04***

3B Develop a self-checking Verilog Test-bench code for the motion detection with the following function. A museum has 4 rooms each with a motion sensor (m0, m1, m2, and m3) that outputs 1 when motion is detected. ***03***

3C Consider the state diagram shown in figure. Analyze the state diagram to determine the shortest input sequence that will distinguish the state transitions. Also verify all state transitions for state 01 and state 11.



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4A Estimate the configurable bits for implementing the circuit shown in Figure Q4A(a) using FPGA. The FPGA layout and CLB details are given the **Fig Q4A (b)**. Determine the generated configuration bitstream for all the configurable elements.

Assume six pass transistors per switch block (SB). Name all the pass transistors in switch block. Accordingly write the bit pattern for switch blocks.

Configuration bits for CLBs		Configuration bits for Switch Box	
CLB0		SB0	
CLB1		SB1	
CLB2		SB2	
CLB3		SB3	
		SB4	

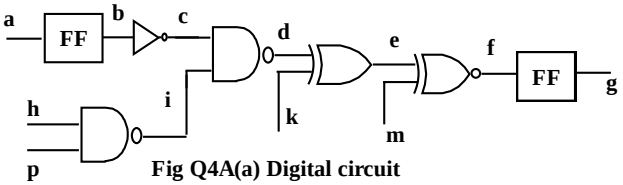
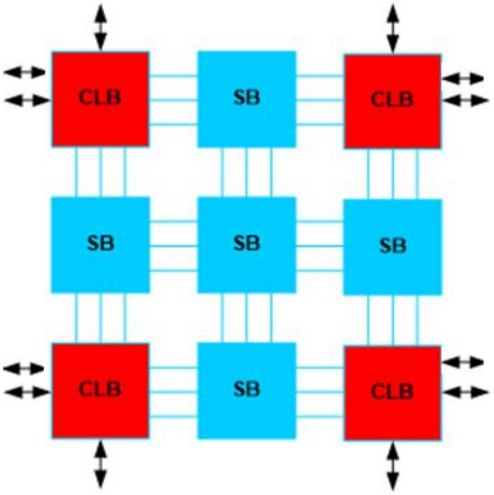


Fig Q4A(a) Digital circuit



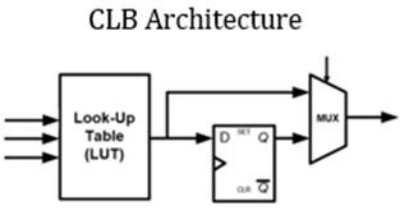


Fig Q4A (b) FPGA Layout

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4B Create a FPGA based circuit to implement 12 input NAND gate. Every CLB of FPGA has the following architectures.

i. 4 numbers of 4 input LUT. Each LUT adds a delay of 100 pico second.

ii. Carry and control Logic

The implemented circuit should have minimum numbers of CLBs and minimum delay. Determine the number of CLBs used and circuit delay. ***04***

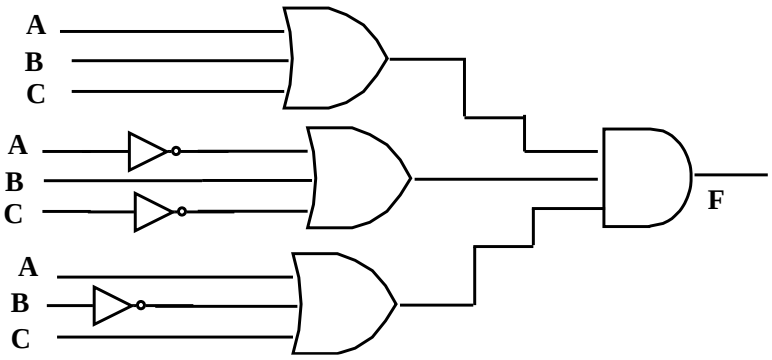
4C Discuss the functionalities of Delay Locked Loop (DLL). ***02***

5A Choose the best LUT to implement the logic circuit given below. Choices available are

(i) 5 input, 1 output LUT with delay of 2 ns

(ii) 6 input, 1 output LUT with delay of 3 ns

Assume 6 transistors are used to implement SRAM cell. ***02***



5B A digital sequential circuit with additional architecture for scan path testing is shown in Fig Q5B. There is stuck-at-1 fault at position H. Choose one of the appropriate present state and input x and explain how stuck-at-1 fault at position H can be detected through additional scan path test architecture shown in Figure. Draw the timing diagram. Mention about the next state of the finite state machine without stuck-at-1 fault and with stuck-at-1 fault at H.

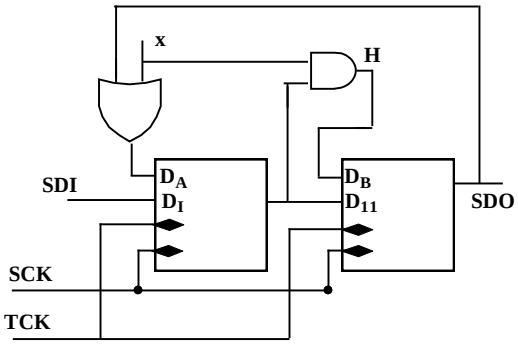


Fig. Q5B

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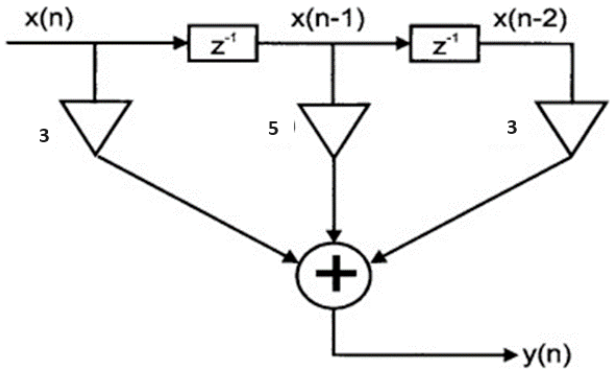
5C Create a FPGA based architecture to implement FIR filter structure shown in the figure. High speed is one of the constraints. Justify the circuit suitability for high speed applications. Also, estimate the output y[2] using the developed FPGA based architecture if x[n]=[**2** 1 3]. Clearly mention the partial output.



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