MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
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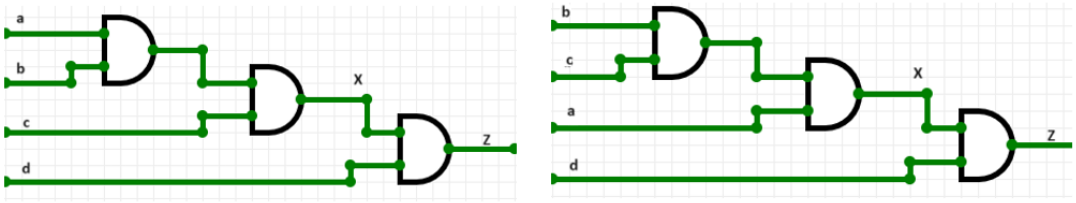
DEPT. OF ELECTRONICS AND COMMUNICATION ENGINEERING
END SEMESTER EXAMINATION MAY 2024 - QUESTION PAPER BLUEPRINT
LOW POWER VLSI – ECE-4063, SET-1

Question No	Topic	Marks
1A	Consider an NMOS transistor fabricated in a 0.18-µm process with L = 0.18 µm and W = 2 µm. The process technology is specified to have C_{ox}=8.6 fF/µm^2, μ_n = 450 cm^2/V.s and V_T=0.5 V. (i) Solve for V_{GS} and V_{DS} that result in the MOSFET operating at the edge of saturation with I_D=100 µA. (ii) If V_{GS} is kept constant, find V_{DS} that results in I_D=50 µA.	5
1B	Construct the ROBDD for the function, F=ab+c. Estimate the output probability using top-down approach.	3
1C	The chip size of a CPU is 15 mm x 15 mm with clock frequency of 500 MHz operating at 4 V. The length of the clock routing is estimated to be twice the circumference of the chip. Assume that the clock signal is routed on a metal layer with width of 1.2 µm and the parasitic capacitance of the metal layer is 1 fF/µm^2. Estimate the power dissipation of the clock signal.	2
2A	Implement the following functions using Footer only sleep transistor logic in single stage. Note: **a'**= complement of variable a. Same for all applicable cases. **F=a+bc (ii) F=a'+b+c (iii) F'= a+c (iv) F'= a'b'+c**	4
2B	Consider the circuits as shown in Figure 2B with different input ordering of P(a)=0.5, P(b)=0.2,P(c)=0.1, P(d)=0.1. Which one has better ordering w.r.t to power dissipation ?  (a) (b) **FIG.2B.**	3
2C	UMC fabrication unit has developed a variation of CMOS chip technology which has transistors with multiple threshold voltages (V_T) to optimize delay or power. It is required to design the aspect ratio, $(W/L)_{SLEEP}$, of sleep transistor for proper operations. Given, V_{DD}=1.3 V, V_{tH}=0.5 V, V_{VGND}=0.2 V, I_{SLEEP}=100 µA, μ_n=250 cm^2/V.s , ε_{ox}=3.9 ε_o, t_{ox}=5 nm. Design for aspect ratio, $(W/L)_{sleep}$, of sleep transistor.	3

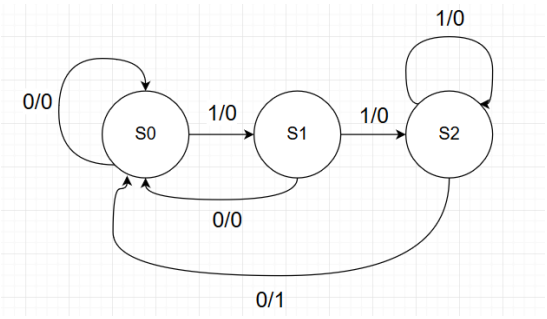
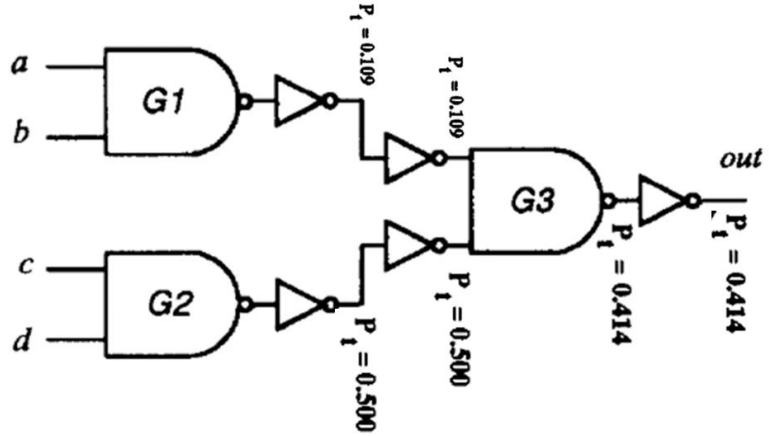
<table>
<tr><td>3A</td><td>The state diagram of a sequence detector and corresponding assignment is shown in Figure 3A & Table 3A. The P_{ij} for S0-> S1 transition is 0.5 and P_{ij} = 0.75 for the rest of the cases. W_{ij}= weight representing activity factor, P_{ij}= probability transition from state s_i to s_j. Estimate (i) W_{ij} (ii) Objective functions (iii) Power dissipation for both assignments, Table 3A. Neglect self-transitions/loop.
 

FIG. 3A.
TABLE 3A.
<table>
<tr><th>State</th><th>Assignment-1</th><th>Assignment-2</th></tr>
<tr><td>S0</td><td>00</td><td>01</td></tr>
<tr><td>S1</td><td>10</td><td>10</td></tr>
<tr><td>S2</td><td>01</td><td>11</td></tr>
</table></td><td>4</td></tr>
<tr><td>3B</td><td>Clocking circuit has 10000 bistables. Collective Buffer is generating clocking signal with a voltage swing of 1.0 V. Given, the aggregate load capacitance per bistable is 12 fF. Also, the drive current follows a triangular waveform during the signal's ramp time of 150 ps.
(i) Estimate the clk current.
(ii) At a clock frequency of 100 MHz, the final inverter stage driving the clock net dissipates power ……</td><td>3</td></tr>
<tr><td>3C</td><td>Mr. X is sending the following set of important serial data (Table 3C) to the base station. It has been observed that a lot of power dissipation is taking place. Calculate the reduced number of transitions, power dissipation, using Weight based Bus invert coding technique on the data sent.
TABLE 3C
<table>
<tr><td>D0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>D1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>D2</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>D3</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>D4</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>D5</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
</table></td><td>3</td></tr>
<tr><td>4A</td><td>A 32-K NMOS static RAM cell using a resistor load is to be designed. Afterwards, it was redesigned using depletion mode transistor. Assume the following parameters: V_{DD} = 2.5 V and $\mu_n * Cox$ = 30 µA/V^2; driver transistors: V_{TND} = 0.45 V and $(W/L)_D$ = 3;</td><td>4</td></tr>
</table>

	load devices: V_{TNL} = −1.0 V, $(W/L)_L$ = 1/3, and R = 1.5 MΩ. Estimate the currents, voltages, and power dissipation in two NMOS SRAM cells.	
4B	Consider the truth table of the Priority function as shown in Table 4B. Construct a precomputation circuit of Priority function. **TABLE 4B.** x_1 x_2 x_3 x_4 | f_1 f_2 f_3 f_4 0 0 0 0 | 0 0 0 0 0 0 0 1 | 0 0 0 1 0 0 1 – | 0 0 1 0 0 1 – – | 0 1 0 0 1 – – – | 1 0 0 0 Truth-Table of a Priority Function	3
4C	In one of logic encoding techniques, one hot encoding is used as redundant code instead of binary code. Design a 3-bit binary code to one-hot coder circuit for low power dissipations.	3
5A	Estimate the total load capacitance of H-tree based clock routing of h=4 levels. Given the total number of clock terminals N=5, the nominal input capacitance at each terminal: Cg=1.3 pF, the unit length wire capacitance: Cw=0.3 pF/µm and the chip dimension: D=4 µm, estimation factor depending on the algorithm used for local clock routing: α=0.11 µm.	4
5B	In a development of ASIC, the circuit shown in Figure 5B is to be mapped with a standard cell library for low power applications. Estimate the optimized mapping w.r.t to minimum area and minimum power mapping.  **FIG.5B** **TABLE 5B**	3

Standard cell	Area(μm²)	O/p Cap.(nF)	I/p Cap.(nF)
INV	928	0.1029	0.0514
NAND2	1392	0.1421	0.0747
NAND3	1856	0.1768	0.0868
AOI21	1856	0.2310	0.0850

5C	Estimate the reduced number of transitions, power dissipation, using SILENT coding technique on the data sent as shown in Table 5C.	3

TABLE 5C

Name	T	T+1	T+2	T+3	T+4
A5	1	1	1	0	0
A4	1	1	1	1	1
A3	1	0	0	0	0
A2	1	0	1	0	1
A1	1	1	0	0	0
A0	1	0	1	1	1

Marks Distribution – Topic wise		**Marks distribution – CO wise**		**Marks distribution - BL wise**	
Topic	**Marks**	**Modified CO**	**Marks**	**BL**	**Marks**
Basic	13	CO1	13	**1**	**-**
Circuit level power reduction	10	CO2	10	**2**	**-**
Logic level power reduction	13	CO3	13	**3**	**30**
Power management	10	CO4	10	**4**	**20**
Clock distribution	4	CO5	4	**5**	**-**

UNDERTAKING: I / we hereby declare that the information regarding this blue print of question paper is circulated only to question paper setting authorities and will be kept confidential.

MIT-Manipal Campus

Faculty Name	DR.SHOUNAK DE			
Role	**Sub Coordinator**			

MIT-Bangalore Campus

Faculty Name				
Role	**Sub Coordinator**			

Date: 14-04-2024