MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

II SEMESTER M. TECH (EMBEDDED CONTROL AND AUTOMATION)
END SEMESTER EXAMINATIONS MAY 2024
VLSI SYSTEM DESIGN (ICE 5412)

Time:3 Hours **09-05 -2024** **MAX. MARKS: 50**

Instructions to Candidates:

- Answer **ALL** the questions.

Q.No.	Description	M	CO	PO'S	BL
1A	Differentiate between enhancement mode and depletion mode transistors.	**3**	**1**	**5**	**4**
1B	An nFET with L=0.5 µm is built in a process where the process transconductance is $100\ \mu A\ /\ V\text{^}2$ and $V_{Tn} = 0.7\ V$. The gate source voltage is set to a value of $V_{Gsn} = V_{DD} = 3.3\ V$. Calculate the required channel width 'W' to obtain a resistance $R_n = 950\ \Omega$.	**3**	**1**	**4**	**3**
1C	Calculate the total capacitance C_{out} of the NOT gate shown in figure 1C with a load capacitance $C_L = 120\ fF$.	**4**	**2**	**4**	**3**

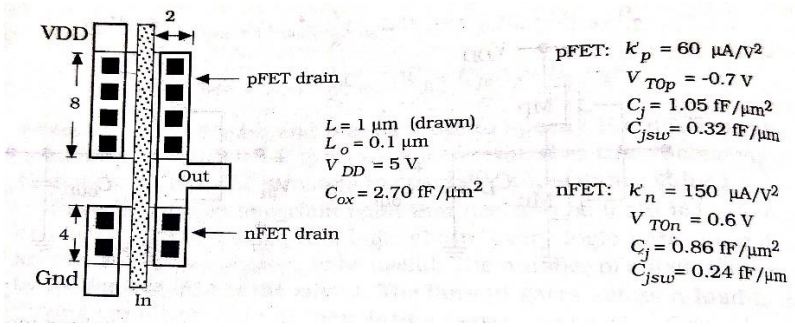

Figure 1C

2A	A CMOS logic gate that implements the function: $f = \overline{(a+b).(b+c).d}$ is needed in a control network. Design the logic circuit with device sizes in the gate that equalize the nFET and pFET resistances. Identify the worst-case nFET and pFET paths that will slow down the response.	**4**	**2**	**4**	**5**
2B	With equations, illustrate how device parameters (any six) of a MOSFET are scaled using the constant voltage scaling model.	**3**	**2**	**5**	**3**
2C	Compare and contrast the working of pass transistors and transmission gates.	**3**	**2**	**4**	**4**
3A	Sketch the transistor-level schematic and stick diagram for implementing the following function: $f = \overline{a.b.c + a.d}$	**3**	**3**	**4**	**3**

3B Consider the two designs of a 2-input AND gate shown in Figure 3B (a) and (b). Justify which of the two circuits will be faster with a calculation of the path effort, delay, and input capacitances x and y to achieve this delay. **4 3 4 5**

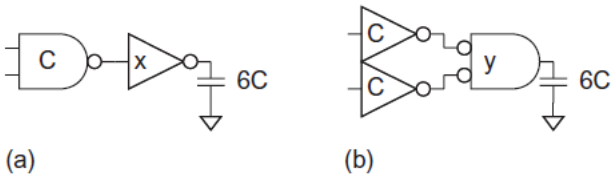

Figure 3B

3C Sketch a transistor level schematic of a pseudo-nMOS gate that implements the function: **3 3 4 3**

$$F = \overline{A(B + C + D) + E.F.G}$$

4A Sketch the transistor level schematic of a clocked JK latch. **3 3 4 3**

4B Implement the following state table using a ROM and two D flip-flops where 'X' is the input and 'Z' is the output and S_0, S_1, S_2 *and* S_3 are the states: **3 4 4 3**

Present State	Next State		Output (Z)	
	X=0	X=1	X=0	X=1
S_0	S_0	S_1	0	1
S_1	S_2	S_3	1	0
S_2	S_1	S_3	1	0
S_3	S_3	S_2	0	1

Draw the block diagram and the ROM truth table.

4C Illustrate different programming technologies of an FPGA with figures. **4 4 5 3**

5A With a flowchart, illustrate the design flow starting from the specification of a chip to its implementation. **4 4 5 3**

5B Compare the three main approaches followed in design for testability in VLSI systems. **3 5 5 4**

5C Interpret the different types of IC packaging techniques that are available in VLSI systems. **3 5 5 3**