Reg. No.



## DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING II SEMESTER M.TECH. (PED & EVT)

## **END SEMESTER EXAMINATIONS, MAY 2024**

## **POWER QUALITY ISSUES & MITIGATION [ELE 5411]**

Timo: 3	Hours Date: 07 May 2024	Max Marke: 50
Instructio	Date: 07 May 2024	
	Answer <b>ALL</b> the questions	
*	Missing data may be suitably assumed.	
1A.	Describe the effects of power quality problems on cu suitable examples and justifications.	stomers with <b>(03)</b>
1B.	A single phase 240V, 50Hz, AC distribution system impedance of $3.1623\angle71.56\Omega$ supplying an industric $Z_L = 10\angle36.86\Omega$ . Determine the voltage across the suitable value of passive compensator element (L rating if a shunt compensator is incorporated to real	has a feeder al load with load. Design or C) and its ize UPF load. <b>(03)</b>
1C.	With the relevant phasor diagram, explain the opera phase three wire capacitor supported DVR to protect loads against voltage sag.	tion of three the sensitive <b>(04)</b>
2A.	Design the value of the shunt compensator to achievoltage regulation across a three-phase three-wire like connected induction motor operating lagging p.f. If from the three phase AC mains with source impedation	eve the zero- balanced star oad supplied ice. (06)
2B.	A three phase four-wire 415 V, 50 Hz AC supply has a 12 kW resistive load connected across line (say R neutral terminal. If it is required to eliminate the neusing a shunt compensator. Design (i) the values of elements (L or C) and (ii) kVA rating of compensator	single phase (-phase) and (-phase) and (-pha
3A.	Based on the types of converters employed, how power filters are classified and which type is genera with proper justifications.	series active ally preferred (03)
3B.	A three-phase three-wire PWM controlled DSTATCC 415V, 50Hz distribution system to provide load b reactive power compensation for unity power fact phase load of 75kVA, 0.8 lagging p.f. load is connect two lines of the system and design the rating of the	M is used at alancing and or. A single- cted between DSTATCOM. <b>(05)</b>

**3C.** With proper justification, explain why an indirect current control approach is superior to direct current control scheme of a DSTATCOM.

- **4A.** A three-phase three-wire 415 V, 50 Hz AC supply feeds power to three-phase delta connected 25kW, induction motor (operating with 0.8pf lagging). If a PWM based 415V, DSTATCOM is used to provide reactive power compensation for UPF operation of motor, design the values of (i) DC bus voltage (ii) DSTATCOM current and (iii) The value of interfacing inductance if the switching frequency is 2.5kHz and ripple current is 15%.
- **4B.** For a three-phase, four-wire VSC based UPQC for the operation of the DSTATCOM and DVR, describe the synchronous reference frame theory-based control algorithm mitigating both power quality problems of voltages and currents with a neat block diagram.
- **5A.** A three phase 415V, 50Hz supply with feeder impedance of  $(1+j4)\Omega/ph$  feeds a balanced star connected load having  $Z_L = (8+j6)\Omega/ph$ . If a PWM based DVR is used to regulate the load voltage to the input voltage (415V), design a) The voltage and current rating of the DVR and b) kVA rating of the DVR
- **5B.** Explain right shunt and left shunt UPQC used for mitigating multiple PQ problems of voltages and currents with neat block diagrams.
- **5C.** For a VSI based three-phase, three-wire UPQC, how are the values of DC bus voltage and capacitor of the VSC of the DSTATCOM estimated?

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