Question Paper

Exam Date & Time: 24-Apr-2024 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
Second Semester Master of Engineering - ME (Microelectronics and VLSI Technology) Degree Examination - April / May 2024

IC Packaging Technology (Elective -II) [MVT 5231]

Marks: 100 **Duration: 180 mins.**

Wednesday, April 24, 2024

Answer all the questions.

1)	With neat figures, illustrate the process flow of through hole packaging and surface mount technology (SMT) packaging along with a real time application. Further, cite the features and limitations of each technique.	(10)
2)	Illustrate differences in the design of a system on chip (SoC) and system in package (SiP) technologies. Support your answer with neat sketches.	(10)
3)	Sketch the various processes involved in realizing a chip on board (CoB) IC packaging.	(10)
4)	With neat figures, illustrate the typical cross-section of a flip chip (FC) package. Further, depict a technique that is used to overcome thermo-mechanical failures in FC packages.	(10)
5)	Sketch a typical anatomy of IC package and depict the physical origin of various parasitics (resistor, capacitor and inductor). Further, depict the factors that leads to the variation in parasitic capacitance and its dependence on the interconnect technology.	(10)
6)	Write at-least two major types of thermal management systems used in modern electronic systems for cooling. Illustrate the physics behind heat dissipation mechanism of the techniques with neat figures.	(10)
7)	Sketch and illustrate the differences between 3D IC stacking with wire bonding and 3D IC stacking with through Silicon via (TSV) technologies w.r.t. form factor and complexity of fabrication.	(10)
8)	Illustrate the anatomy of a bumped die depicting (i) front end of the line (FEOL), (ii) local interconnects, (iii) back end of the line (BEOL), and (iv) bump along with their typical functionality in a typical IC.	(10)
9)	Sketch the differences between package on package (PoP) technology and chip stacking by wire bonding technology for realizing 3D ICs.	(10)
10)	With neat figures, illustrate the wafer level packaging technology for 3D IC realization. Further, compare the 3D IC realized with wafer level packaging technology with a flip chip technology IC and lead frame technology IC	(10)

w.r.t. its form factor.

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