Question Paper

Exam Date & Time: 23-Apr-2024 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
Second Semester Master of Engineering - ME (VLSI Design / Microelectronics and VLSI Technology) Degree Examination - April / May 2024

Low Power VLSI Design [VLS 5202]

Marks: 100 **Duration: 180 mins.**

Tuesday, April 23, 2024

Answer all the questions.

1)	Explain the need to be concerned about the power dissipation in VLSI chips. [L2, CO-1]	(10)
2)	Describe the various leakage current components in a CMOS chip. Explain each of them briefly with relevant diagrams. [L2, CO-1]	(10)
3)	Explain with the help of a diagram, the technique of artificial stacking of transistors (LECTOR) to control the sub-threshold leakage current. [L2, CO-2]	(10)
4)	Discuss the following techniques of achieving multiple threshold voltages: [L2, CO-2] a) Multiple channel Doping (5) b) Multiple Oxide CMOS (MOXCMOS) Circuit (5)	(10)
5)	Briefly explain the two Dynamic V_{th} scaling techniques with relevant diagrams. [L2, CO-2]	(10)
6)	a) The chip size of a CPU is 1.5cm×1.5cm with clock frequency of 600MHz operating at 1.5V. The length of the clock routing is estimated to be thrice the circumference of the chip. Assume that the clock signal is routed on a metal layer with width of 800nm and the parasitic capacitance of the metal layer is 2fF/µm2. What is the power dissipation of the clock signal? (5) [L3, CO-2] b) Calculate the clock signal power in the low power mode of the CPU in which the operating voltage is 1.1V and the clock is disabled 60% of the time. (5)	(10)
7)	Explain with diagrams, the Reliability-Driven Voltage Scaling approach for dynamic power reduction. [L2, CO-3]	(10)
8)	What is a glitch? Why it is important to minimize glitch power? What are the two categories of glitches? Explain with diagrams. (3+3+4) [L2, CO-3]	(10)
9)	Describe combinational and sequential clock gating approaches. [L2, CO-3]	(10)
10)	Discuss the levels of granularity of the circuit block at which clock gating is applied. [L2, CO-3]	(10)

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