Question Paper

Exam Date & Time: 29-Apr-2024 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
Second Semester Master of Engineering - ME (VLSI Design / Microelectronics and VLSI Technology) Degree Examination - April / May 2024

Advanced VLSI Design [VLS 5201]

Marks: 100 **Duration: 180 mins.**

Monday, April 29, 2024

Answer all the questions.

1)	a) Explain the effect of Temperature and Voltage on CMOS capacitor. (06 marks) b) For a 1pF poly1-poly2 capacitor at room temperature (27°C), estimate the minimum and maximum capacitance over a temperature range of -40 to 100°C. [Data Given: TCC = 20ppm/°C] (04 marks)	(10)
2)	Discuss the different types of MOSFET parasitic capacitance that show up at high frequency? Explain with a model.	(10)
3)	With the help of a diagram, explain the working of a simple current mirror. Derive the relationship between the reference current and the output current.	(10)
4)	Explain the working of regulated cascode current mirror with a neat schematic and a small-signal model.	(10)
5)	With the help of a schematic diagram and a small-signal equivalent circuit, develop an expression for the small-signal incremental voltage gain, A_V of a CMOS Common-Source amplifier with passive resistor load.	(10)
6)	a) With the help of a diagram, explain CMOS Common-Source amplifier with current source load. (06 marks) b) Calculate the small-signal voltage gain, A_V, for the circuit shown below. Assume that M1 is biased in saturation and I1 is an ideal current source. [Data: K_n = 50µA/V², W = 10µm, L = 5µm, V_{GS} = 1.2, V_{th} = 0.856, r_0 = 1.7MΩ] (04 marks)	(10)

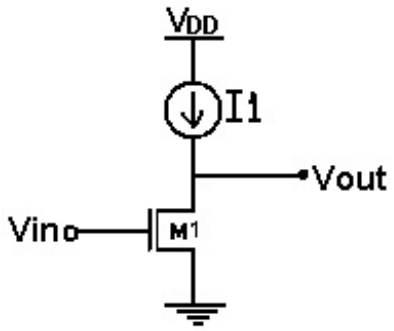

Fig. 6 (b)

7)	Explain, with the help of a neat schematic diagram, a bandgap voltage reference. List the advantages of this circuit over other simple references?	(10)
8)	Explain, with an example, how to make switched-capacitor circuits insensitive to stray	(10)

	capacitances?	
9)	List the issues involved in mixed-signal layout? Discuss each of them briefly.	(10)
10)	With diagrams, explain the principle of working of the Two-Step Flash ADC. What are the accuracy issues related to it?	(10)

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