Question Paper

Exam Date & Time: 04-Jun-2024 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
Second Semester Master of Engineering - ME (VLSI Design / Microelectronics and VLSI Technology) Degree Examination (Makeup Exam) - June 2024

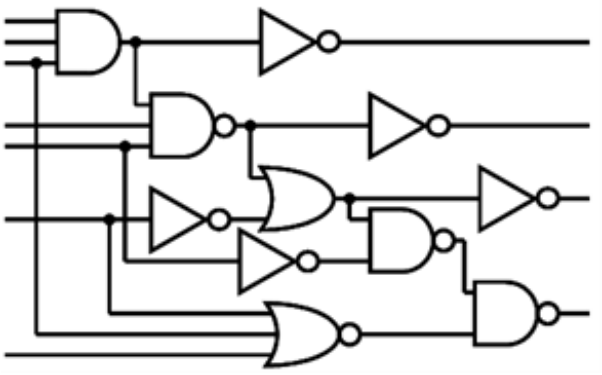
Low Power VLSI Design [VLS 5202]

Marks: 100 **Duration: 180 mins.**

Tuesday, 04 June 2024

Answer all the questions.

1)	Derive an expression for the short-circuit power dissipation component in a CMOS circuit. Analyze the effect of output load capacitance on the short-circuit current. [L4, CO-1]	(10)
2)	Explain the following techniques for leakage reduction: (3+3+4) [L2, CO-2] a) Multiple channel doping b) Multiple body bias c) Super cut-off CMOS (SCCMOS)	(10)
3)	Explain with diagrams, the following multiple V_{th} techniques to suppress the sub-threshold leakage current: [L2, CO-2] Multi-threshold CMOS (MTCMOS) (5) Dual threshold CMOS (5)	(10)
4)	The following circuit is designed in a CMOS technology using low threshold transistors. Each gate has a delay of 4ps and a leakage current of 12nA. Given that a gate with high threshold transistors has a delay of 15ps and leakage of 2nA. [L3, CO-2] a) Optimally design the circuit with dual-threshold gates to minimize the leakage current without increasing the critical path delay. What is the percentage reduction in leakage power? (5) b) What will the leakage power reduction be if a 25% increase in the critical path delay is allowed? (5)	(10)



5)	Explain with relevant diagrams, the Voltage Scaling through Optimal Transistor Sizing approach for dynamic power reduction. [L2, CO-3]	(10)
6)	Model and explain with the help of neat diagrams, the Architecture-Driven Voltage Scaling technique by trading area for lower dynamic power through hardware duplication. [L3, CO-3]	(10)
7)	Explain the various ways of glitch reduction with relevant diagrams. [L2, CO-3]	(10)
8)	Describe the combinational and sequential clock gating methods. [L2, CO-3]	(10)

9)	Discuss the effects of clock latency and skew in the context of clock gating. [L2, CO-3]	(10)
10)	Explain the system design issues with multi-voltage designs. [L2, CO-3]	(10)

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