Question Paper

Exam Date & Time: 30-Apr-2024 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
Second Semester Master of Engineering - ME (VLSI Design / Microelectronics and VLSI Technology) Degree Examination - April / May 2024

Physical Design Elective -2 [VLS 5234]

Marks: 100 **Duration: 180 mins.**

Tuesday, April 30, 2024

Answer all the questions.

1) Differentiate two input NOR and NAND gate circuit using CMOS logic. Explain their transistor sizing considering a reference inverter of size 3/1. (10)

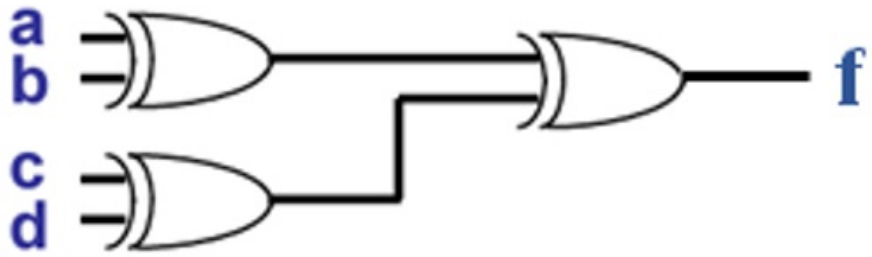
CO - 1, BT-4, Marks-10

2) Distinguish dynamic logic from static CMOS logic including suitable examples (10)

CO - 1, BT-4, Marks-10

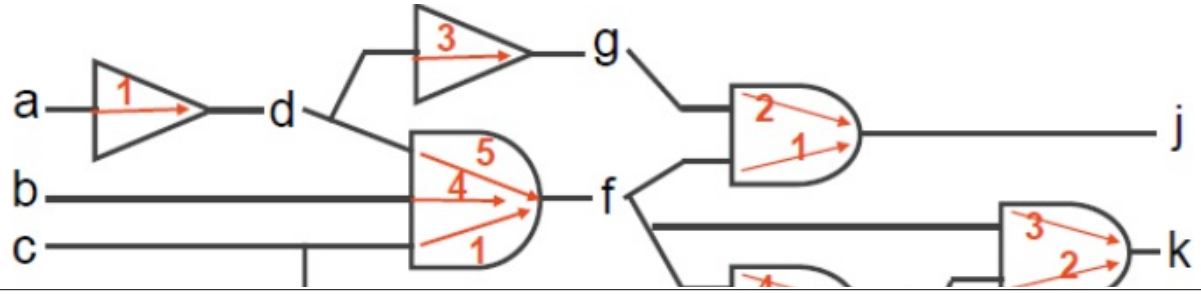
3) Implement reduced order binary decision diagram for the circuit given below (10)

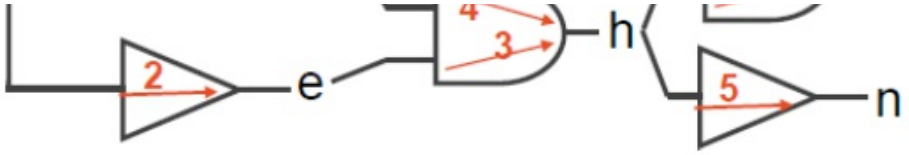
CO - 2, BT-3, Marks-10



4) Examine whether the following circuit meets a timing cycle = 11? Show the different steps to calculate Arrival Time, Required Arrival Time, and Slack. (10)

CO - 3, BT-4, Marks-10





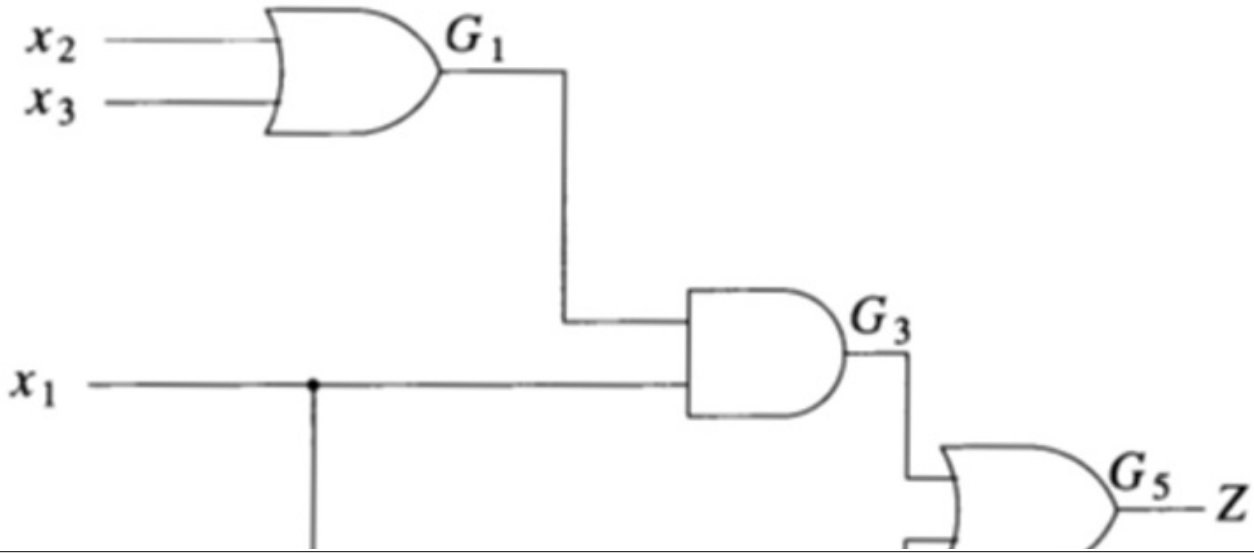
5) Sketch height and width of ASIC and Core logic. Describe clock planning. (10)
CO - 3, BT-4, Marks-10

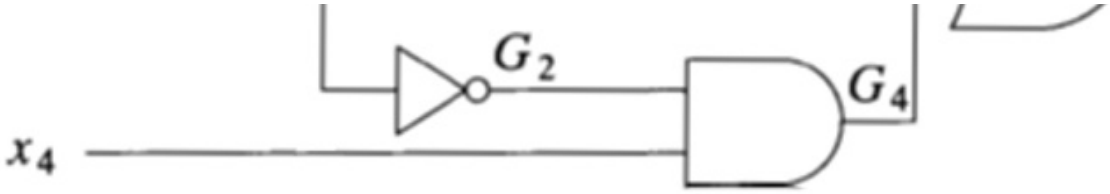
6) List the objectives of routing? Explain Source to sink, Minimum spanning tree and Half-perimeter methods in routing with suitable examples CO - 4, BT-2, Marks-10 (10)

7) Explain the different types of capacitances considered in the extraction procedure after the layout? CO - 4, BT-2, Marks-10 (10)

8) Differentiate between verification and testing. Compute the probability of fault in a system with 10 million transistor and the probability of fault of individual transistor is 0.1 micron CO - 5, BT-4, Marks-10 (10)

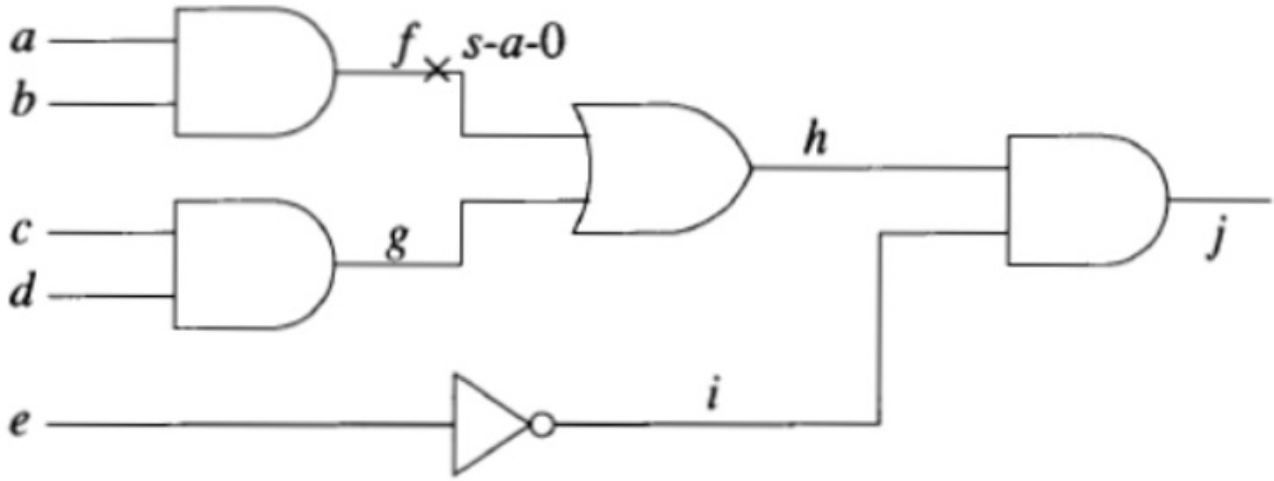
9) Solve for the input vectors for detecting the stuck at faults using faulty expressions for (a) x1 stuck at 0 (b) x2 stuck at 1 (10)
CO - 5, BT-3, Marks-10





10) Solve for the test vector for the s-a-0 shown using D algorithm (10)

CO - 5, BT-3, Marks-10



-----End-----