Question Paper

Exam Date & Time: 02-May-2024 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

Manipal School of Information Sciences (MSIS), Manipal
Second Semester Master of Engineering - ME (VLSI Design) Degree Examination - April / May 2024

Universal Verification Methodology [VLS 5204]

Marks: 100 **Duration: 180 mins.**

Thursday, May 02, 2024

Answer all the questions.

1)	Explain the following Object Oriented Programming Concepts with short code examples. Also, apply your understanding of these terms to relate how these concepts are applicable in UVM. a. Inheritance b. Parameterization	(10)
2)	Illustrate and describe the different UVM phases with a neat diagram.	(10)
3)	In the context of a UVM sequence, explain about m_sequencer and p_sequencer. Additionally, demonstrate how to set a default sequencer.	(10)
4)	Analyze the challenges associated with reset handling in a verification environment. Specifically discuss how reset handling is implemented in a monitor, illustrating your points with brief code snippets.	(10)
5)	Given a basic test 'base_test' that defines specific testbench configuration parameters and initiates 'my_seq' in its run_phase, apply your understanding to construct a derivative test. Include detailed code snippets that illustrate how a different sequence can be launched.	(10)
6)	Explain configuration mechanisms. Compare create () and new () methods in UVM.	(10)
7)	Describe implementing a coverage model.	(10)
8)	What is a UVM Virtual Sequencer and when do we need one?	(10)

Demonstrate the use of a virtual sequencer in a UVM testbench by using code snippets for the same.

9) What is the UVM RAL model? Examine and explain the different RAL building blocks. (10)

10) What is TLM Analysis port? Examine the concept of TLM analysis ports and provide code examples demonstrating how to declare an analysis port and connect it with its implementation. (10)

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